論 文

기가주파수대 멀티플렉서 설계에 관한 연구

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Study of the Multigigabit Multiplexer Design

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要 約 갈륨비소를 사용한 SCFL을 채택하여 4:1 시분할 멀티플렉서를 설계하였다. 설계된 멀티플렉서는 2:1 시분할 주파수 분할기를 사용하여 2:1 멀티플렉서 2단을 사용하였다. 시뮬레이션 결과, 최고 동작 주파수는 6.25 GHz이었고 전력소모는 192mW이었다. 따라서 최대 출력 bit 율은 12.5 Gbit/sec를 얻었다. 이 결과는 기존의 멀티플렉서에 비해 속도 및 전력소모 면에서 상당히 개선된 것이다.

ABSTRACT A 4:1 Time Division Multiplexer(MUX) had been designed in using GaAs Source Coupled FET Logic (SCFL). Designed Multiplexer uses a time division frequency divider and two stage of signal combining 2:1 multiplexer. The performance of the multiplexer is verified by PSPICE simulation. Designed circuit operates up to 12.5 Gbit/s with a power dissipation of 192mW. These performance are more advanced than other reported multiplexer in the speed and power dissipation.

1. INTRODUCTION.

Recently digital transmission systems have made rapid progress toward high capacity and high speed. The data transmission rate has entered into the multigigabit range. So a time division multiplexer is a very important block for high speed data manipulation.

For these high speed digital systems, GaAs digital ICs are needed. This circuit was developed for high speed fiber optic application, where output data must have very low jitter at data rate in the gigabit range and input data is most likely to be ECL or ECL compatible format.

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Therefore output data must be retimed with a flip flop and SCFL circuit is suitable to GaAs metal semiconductor FET(MESFET) IC / LSI because of its small Cgd, threshold voltage(Vth) tolerance, high switching and low power dissipation[1] [2] [3]

2. CIRCUIT DESIGN

2.1 Basic logic unit

GaAs ICs are composed of normally on or / and normally off MESFETs. Typical normally on ICs are BFL[4] and SDFL[5] etc.

One of the well known normally off IC is DCFL[6]. But this circuit has two major disadvantages ; one is the small Vth margin and the other is a small drive capability against heavy loads of fan-outs and interconnection.

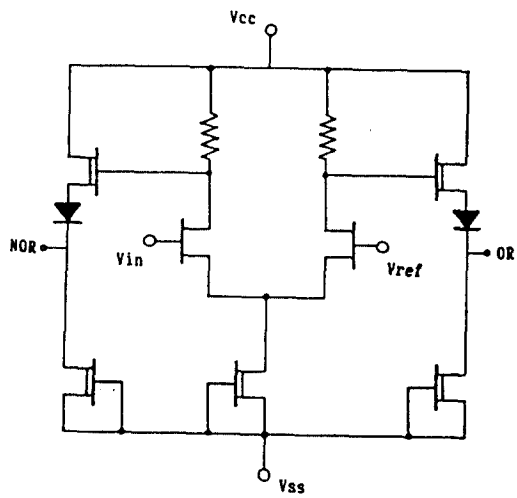
To improve a weak point in DCFL LPFL[7] is proposed SCFL[1] [2] [3] etc.

To realize high speed, in GaAs ICs with these conventional circuit configurations, the MESFET gate length must be reduced to submicron dimension. However, a fabrication process for GaAs ICs composed of submicron gate MESFET is not complete.

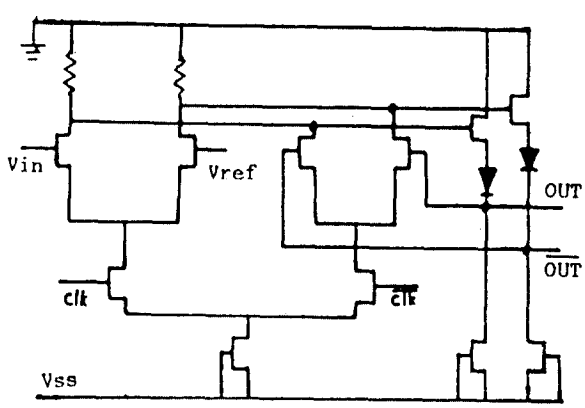
In addition to gate length, one of the factors which have effects on both propagation delay time and transition time is gate to drain capacitance Cgd. This capacitance is reduced with an increase in drain to source voltage Vds[8]. But in conventional circuit it is difficult to reduce Cgd sufficiently.

The reason is that Vds for driver FET only sets logic swing voltage and must be lower than the pinch off voltage when an FET is switched on.

On the other hand, these bias points are adjustable in current mode logics(CML) circuits. This GaAs CML is called a Source Coupled FET Logic(SCFL). The configuration of the designed SCFL OR / NOR gate and delayed flip flop(D-FF) ars shown in Figure 1 and caculated results is shown in Figure 2 Which is simulated by PSPICE[9].

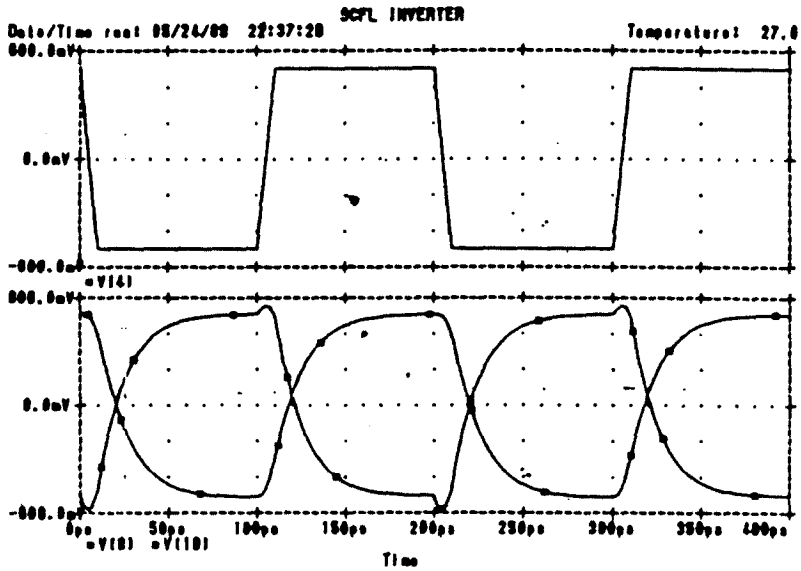


(a) OR / NOR gate.



(b) Delayed flip flop.

Fig. 1. Designed schematic diagram of SCFL.



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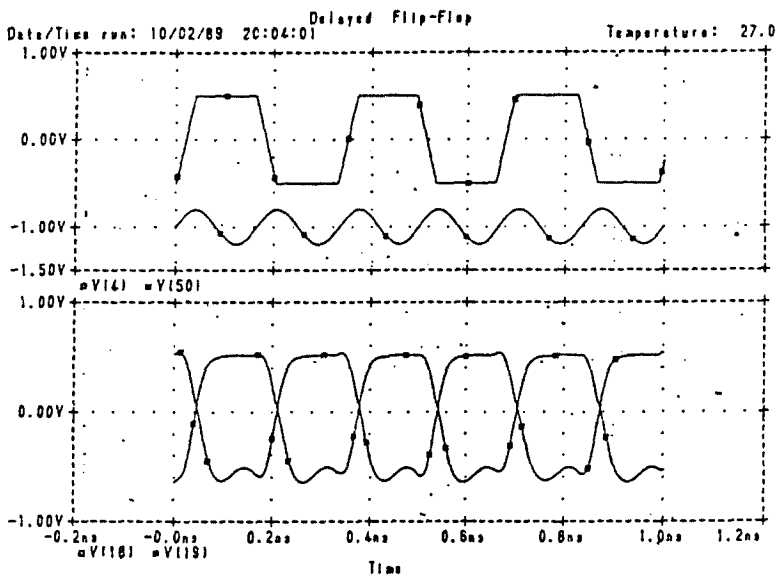


(b) Delayed flip flop.

Fig. 2. Calculated output characteristics of designed circuit.

2.2 Frequency Divider.

The most important circuit for creating a multiplexer is the flip flop circuit. The maximum operation frequency of the MUX is

determined by the FF circuit[10].

Therefore a frequency divider realized by a Master Slave delayed flip flop(MS D-FF) has a important role in MUX. Maximum output bit rate is defined by the delay time between Master and Slave. Delay timeΔt is equal to the bit widthΔt and 1/2 fmax. The configuration of the 2:1 frequency divider is shown in Fig. 3.

In the Master Slave D-FF the data are amplified by Master stage during negative clock periods and the data are generated by Slave stage after two clock cycles. The operations are controlled at a half clock rate[11][12]. The caculated output of the 2:1 frequency divider is shown in Fig. 4

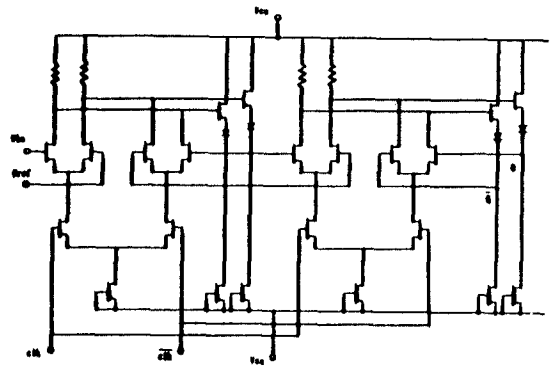


Fig. 3. Clocked MS-D-FF using SCFL.

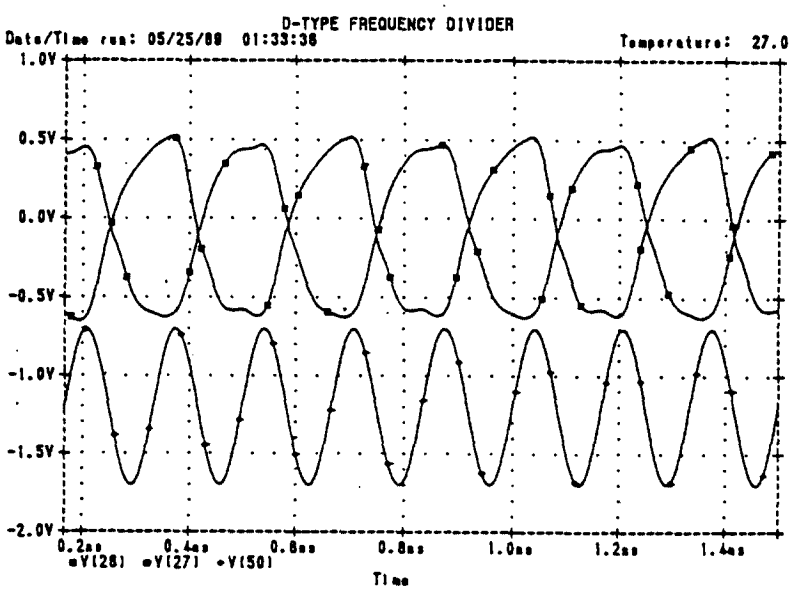


Fig. 4. Caculated output of the designed 2:1 frequency divider.

3. ARCHITECTURE

There are 3 options for achieving high speed multiplexing that have been considered.

One option is to generate a shift register that loads data parallel for one clock cycle and

then shifts it down the register for the three clock cycles[13] [14] [see Fig. 5(a)].

This architecture has the advantage that it inherently retimes the data at the output. It is most common approch in GaAs.

The major disadvantages of this architecture are in requirement for high speed clock and the fact that 3 level serise gated logic must be used in the speed limiting path.

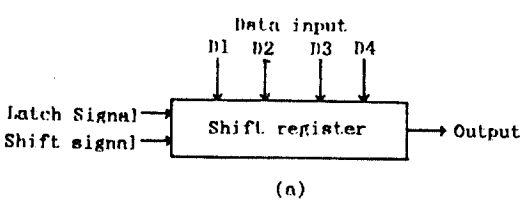
The second option[see Fig. 5(b)] is to have a divice which loads all data in parallel and then combines all four channels into single channel using an asynchronous 4 bit MUX gate structure with timing signals generated separately for the select lines[10] [15][16].

To generate retimed data that output of the channel combining circuit be followed by a flip flop. The down side of this architecture is that speed of operation is likely to be limited by the speed of the output flip flop and delay line and not the 3 level series gated structure.

It should therefore be possible to archieve a higher speed in this architecture than in the first option assuming that ploblem of providing a high speed delay line can be solved.

A third option involves loading the 4 bits in parallel and then following this by two stage of signal combining[i, e, two two-one MUXes in series. see Fig.5(c)]. This type of approach can potentially achieve an extremely high data rate because the ECL two to one MUX blocks can be only two level series gate[17][18].

The time slots of the output bit stream are defined only by the sinusoidal select signal and the bit widthΔt is half the clock period.



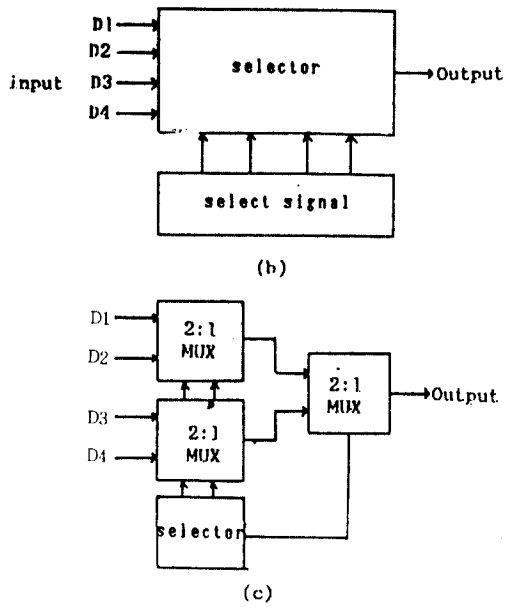


Fig. 5. Three alternative architecture.

So we decide upon the architecture that of option #3. Simulation verified that option #3 obtains double data rates compare to other option. Schematic waveform of select signal for cyclical selection of four data chan nels and logic diagram of 4:1 MUX are shown in Fig. 6.

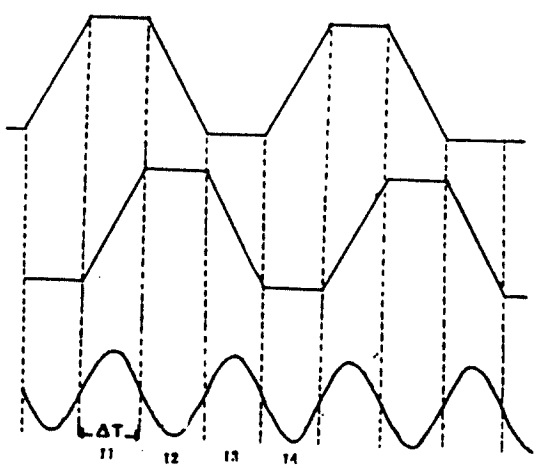
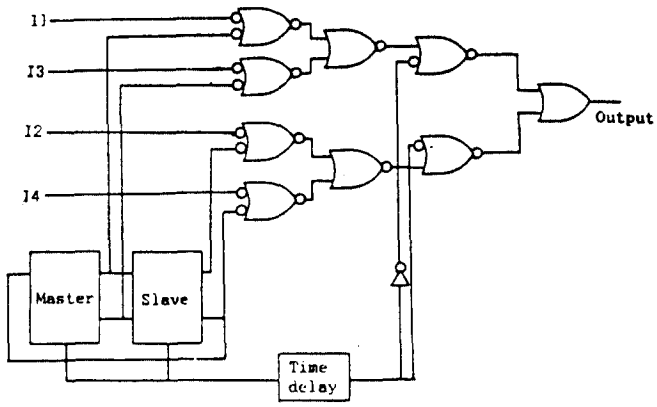


Fig. 6. (a) Schematic waveforms of the three signals for cyclical selection of four data channel.



(b) Logic diagram of the designed MUX

4. RESULTS AND FUTURE DIRECTION.

The caculated output of designed 4:1 MUX is shown in figure 7 and performance summary is shown in table〈1〉. Functional die have toggled in response to a standard DC input pattern to a frequency of 6.25GHz and confirmed to theoretical caculation $f_{max} = 1/2\Delta t$. Therefore maximum output bit rate is 12.5 Gbit/s.

This speed is faster than that of reported at date and power dissipation is 192 mW, which is less then that of other 4:1 MUX [4] [13] [17].

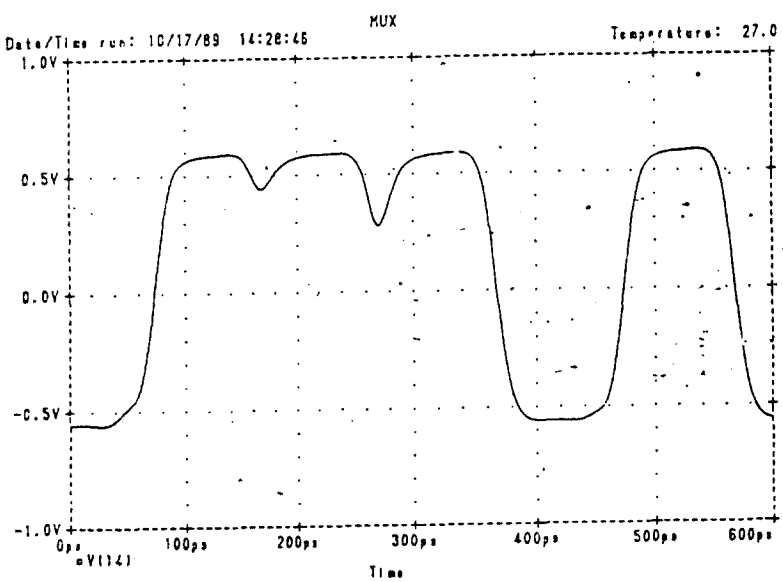


Fig. 7 Output of Designed 4:1 MUX

Table 1 Performance Summary

Item	4:1 MUX
Gate Length	1um
Unit Logic Circuit	SCFL
Clock frequency(max)	6.25 GHz
Input voltage swing	1 Vp-p
Output voltage swing	1 Vp-p
Total power dissipation	192 mW
Maximum output bit rate	12.5 Gbit / s

However there are a number of specific thing which can be done to increase performance. One thing is to more carefully choose and optimize divices for use in circuit.

Better characterizion and modeling of parasitic package and substrate effects will allow better optimization. Beyond this it will be necessary to develope to more rigorously charactrize interconnect and to develope models more suitable for high frequencies. Technical progress in fabrication(ex. advanced SAINT, submicron, airbridge) is to be applied to simulation parameter.

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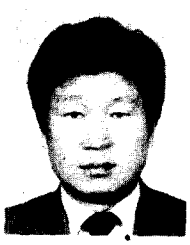

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