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DAMA-SCPC 시스템을 위한 초고주파 주파수 합성기의 설계 및 분석

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Design and Analysis of Microwave Frequency Synthesizer for DAMA-SCPC System

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要 約

본 논문에서는 무궁화 위성을 이용하여 음성전화 및 저속 데이타 서비스를 제공하는 DAMA-SCPC 시스템에 사용될 낮은 위상잡음 특성을 갖는 초고주파 주파수 합성기의 설계 및 분석에 관해 상세히 다루었다. 설계된 초고주파 주파수 합성기는 4개의 모듈 즉, 125MHz 디지탈 위상 동기 발진기, 875MHz 아날로그 위상 동기 발진기, 14배 주파수 체배기 그리고 13GHz 디지탈 위상 동기 주파수 합성기로 구성되었다. 13GHz 주파수 합성기에 대하여 광대역 전압 제어 발진기의 비선형성과 분주비의 변화에 의한 영향을 없애기 위하여 위상 동기 루프의 이득을 제어하는 회로를 고안하였으며, 부궤한 루프의 안정도와 출력의 위상 잡음을 정확하게 예측하기 위하여 회로내에 포함된 모든 부품의 특성을 고려하는 새로운 설계 방법을 상세히 기술하였다. 본 논문에서 제안된 정확한 수식을 갖고서 예측된 위상잡음 성능은 위상잡음 측정 시스템을 사용하여 측정된 성능들과 비교할때 약 2dB 의 작은 오차를 보였다. 설계된 주파수 합성기의 13.555GHz 출력 주파수에 대해 30KHz offset 에서의 위상잡음은 -88dBc/Hz 였으며, 또한 30Hz 에서 30KHz offset 까지 적분된 위상잡음은 0.96rms degrees 이었다. 500MHz 주파수 합성 대역에 걸쳐 주파수 합성기의 공칭 출력 전력은 13dBm 이며, 그 출력 평탄도는 $1dB_{(p-p)}$ 이었다.

ABSTRACT

This paper presents the design and analysis on a microwave frequency synthesizer with low phase noise characteristic utilized in DAMA-SCPC system which shall provide telephone service and data service with low transmission rate through the KOREASAT. The designed microwave frequency synthesizer is composed of four modules which are the 125MHz digital PLO,

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875MHz analog PLO, X14 frequency multiplier and 13GHz digital PLL synthesizer, respectively. In the wideband 13GHx PLL frequency synthesizer, for overcoming the effcets due to voltage controlled oscillator(VCO) nonlinearity and division ratio variations, the circuit to control the loop gain is contrived. The new design approach to consider the effect for all components included within circuits is proposed and described in detail for the purpose of the accurate estimation of the loop stability of PLL and output phase noise.

The estimated phase noise performances with the exact formula proposed on this paper are compared with those measured by the phase noise measurement system, and the compared result shows the difference as low as 2dB. At 13.555GHz, the SSB phase noise of the designed synthesizer is as low as -88dBc/Hz at 30KHz offset, and also the integrated phase noise over 30Hz to 30KHz offset is 0.96 in rms degrees. The nominal output power of the synthesizer is 13dBm, and its flatness over 500MHz tuning band is $1dB_{(p-p)}$.

I. INTRODUCTION

The use of phase locked loop(PLL) frequency synthesizers in communication, measurement, and radar systems has been growing steadily because of their many advantages, especially frequency selection with digital commands and predictable frequency stability due to an external reference signal. Although all synthesizers share common features, they exhibit significant differences as a result of specific system requirements and/or specific applications. In the satellite communications, these synthesizers are required as carriers for increasingly sophisticated baseband information, or as local oscillators for achieving frequency conversions from/to carriers to/from satellite transponder frequency. Because the phase noise on the microwave local oscillator has directly the influence on a digitally modulated carrier and the integrated phase noise in the double sided nyquist bandwidth increases the bit error rate(BER) of PSK systems[1-4], it must be designed to have low phase noise performance in digital satellite communication system. Therefore, the phase noise specifications for it of each system need to be considerd according to transmission rate per carrier. That is to say, in case of DAMA-SCPC system with low transmission rate, the phase noise performance at small offset from a carrier is more important than it at large offset.

Recently, a microwave frequency synthesizer of MMIC technique was developed owing to semiconductor technology[5-7], but isn't yet available on the system application to require low phase noise performance due to high phase noise performance of a (Voltage Controlled Oscillator(VCO). In order to obtain required frequency step size and low phase noise characteristic of PLL synthesizer in available satellite communication systems, it is designed with a few PLLs which mix two type, analog and digital, and is designed with the technique which converts a signal fed from a microwave VCO to a L-band signal for overcoming the operational range of a frequency divider and decreasing noise floor of a reference signal and phase detector by division ratio[7-11]. Also, since the phase noise can be accurately estimated owing to contri-

butions of Robins and Kroupa[4,8,9], the optimal design which considers size, cost and performance of a synthesizer is possible in order to meet required phase noise specifications.

In this paper, for overcoming the effect due to VCO nonlinearity and divider variations, an the circuit to control the PLL loop gain is contrived. The design approach to consider practical values of all components included within circuits is proposed, and the loop stability analysis and the phase noise estimation are in detail performed. Based on the proposed approach, the microwave frequency synthesizer with low close-in phase noise performance has been developed for the purpose of being used in DAMA-SCPC System which will perform voice & data services with low traffic density as a sort of earth station using the KOREASAT.

II. SYSTEM REQUIREMENTS

Since the performance of a coherent digital modulation system is degraded by an excessive amount of the phase noise, the phase-noise requirements of the signal sources often become the limiting factor for the overall system. In general, the sideband phase noise can be the cause of interference into the information bandwidth and can limit the overall system sensitivity[1,2]. Considering the phase noise sources as independent random variables, the resultant equivalent phase noise pdf(probability density function) approaches a normal or gaussian curve since the number of individual sources is large. The phase noise is added with the channel noise within the specified bandwidth to produce that a total carrier-to-noise ratio is given by[2,3]

$$\left(\frac{C}{N}\right)_{Total} = \frac{1}{\left(\frac{C}{N}\right)_{Channel}^{-1} + \left(\frac{C}{N}\right)_{Phase}^{-1}} \quad . \quad (1)$$

where,

$\left(\frac{C}{N}\right)_{Total}$ = *total C/N caused by channel noise plus phase noise*

$\left(\frac{C}{N}\right)_{Channel}$ = *C/N caused by total channel noise in the link*

$\left(\frac{C}{N}\right)_{Phase}$ = *C/N caused by total phase noise in the link*

It is suggested that in many systems an economic analysis will show that if the link degradation caused by the phase noise exceeds 0.4 dE it will be cheaper to reduce the phase noise itself than to improve it by increasing the EIRP or G/T[4,9]. The spurious phase jitter may be introduced by each local oscillator used for the frequency conversion and also by the AM-PM effects resulted from each high power amplifier in the satellite communication link.

The phase noise specifications that is required in communication system using PSK modulation technique depend on the carrier recovery loop and BER of a coherent demodulator[4]. The phase error, which is resulted from the phase noise density coming into the carrier recovery loop, is determined by the error response, transfer function and related offset frequency of that loop, and is largest in neighborhood of the natural frequency. From the view point of BER, the phase noise coming into a coherent demodulator brings about the phase difference between an input signal and a carrier. This, the phase difference, depends on the error response and noise bandwidth of the carrier recovery loop. Therefore, it can be summarized that the phase noise specification at low offset frequency depends on the carrier recovery loop and by up to high offset frequency of the

double sided bandwidth depends on a coherent demodulator.

The requirement for the phase noise performance in the microwave synthesizer design of DAMA-SCPC system with the double sided bandwidth of about 30KHz is shown in Fig. 1 along with the IESS-308 specification[12].

III. FREQUENCY SYNTHESIZER DESIGN

The practical design approach to consider the effect for all components included within circuits is proposed for the purpose of the accurate estimation of the loop stability and phase noise. The designed microwave frequency synthesizer is composed of four modules which are the 125 MHz digital PLO(phase locked oscillator), 875 MHz analog PLO, frequency multiplier(X14) and 13 GHz digital PLL synthesizer, respectively, as shown in Fig. 2. Since the first, second and third module is necessary to generate two reference signals for the fourth module which is the third PLL synthesizer, the prcatical design approach proposed in this paper is limited and described in detail for only the third PLL synthesizer. But, the detailed internal configurations of each module are briefly explained as follows.

The 125 MHz digital PLO module of the first PLL is used to clean an external 10 MHz reference signal received through long distance from an indoor unit by a crystal filter, and to generate the 125 MHz signal locked to

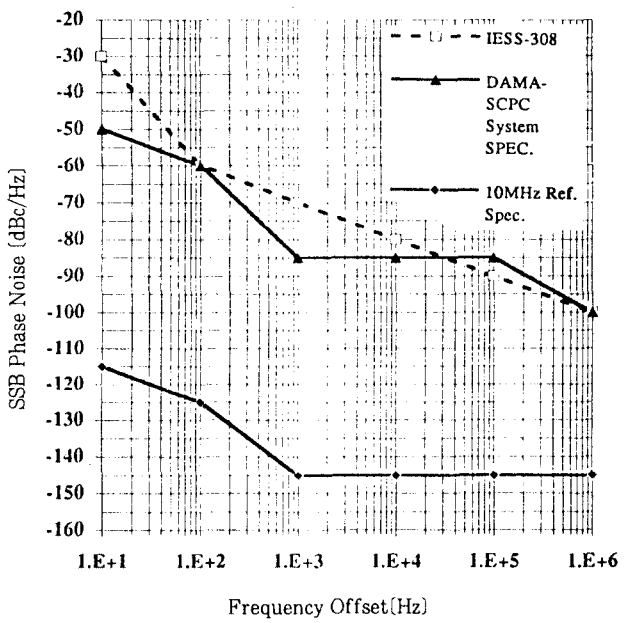


Fig. 1. The SSB phase noise specification of the microwave synthesizer (DAMA-SCPC system)

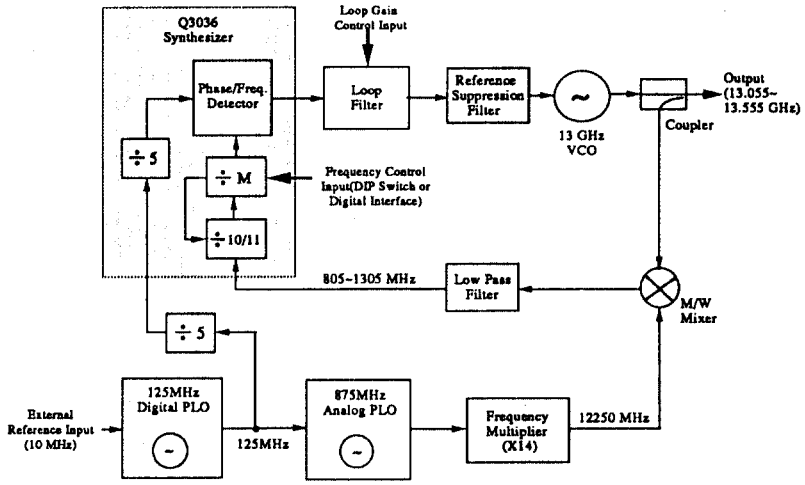


Fig. 2. The architecture of the microwave synthesizer

it. It is a digital PLL with 100 Hz loop bandwidth and consists of a Q3036 frequency synthesizer IC supplied by Qualcomm, the active loop filter, the reference suppression filter and the 125MHz VCXO(voltage controlled crystal oscillator).

The 875MHz analog PLO module of the second PLL is used to generate the 875MHz signal locked to the 125MHz reference signal source. It is the analog PLL with about 20KHz loop bandwidth and consists of a sampling phase detector, the 875MHz VCO with very low phase noise characteristic, the lag-lead loop filter and the auto-search circuit.

By the designed frequency multiplied module, the output signal of the 875MHz analog PLO is frequency-multiplied to the 12.25GHz signal by using the SRD(step recovery diode) harmonic generator followed by the waveguide band pass filter with about 40MHz bandwidth.

In the digital frequency synthesizer module of the third PLL, the 12.25GHz signal coming from the frequency multiplier module is mixed by the double-balanced mixer with the signal coupled with the extent of about 8dB from the 13GHz VCO output(13.055~13.555GHz) in order to yield the IF signal(805~1305MHz). And then, that IF signal will be divided into 161 to 261 by a divider according to the frequency selection. In the digital phase detector, it is compared with the reference signal coming from the 125MHz PLO module.

The assumption of linearity allows the loop to be treated as a control system and modeled via Laplace transform approach. The fourth module, the 13GHz digital synthesizer, can be

modeled as a PLL feedback control loop as shown in Fig. 3. The phase detector gain, K_ϕ, for the Q3036 is 0.302V/rad, and in this design a second order type PLL is assumed, that is, it has two perfect integrators (poles on the imaginary axis). The tuning voltage-to-frequency conversion of the VCO implements integration with respect to phase, and the other integrator is given from an active loop filter. The I/O transfer characteristic of the microwave VCO is shown in Fig. 4. The VCO is fabricated on the allumina hard substrate and designed with a GaAs power FET chip(FLK022XV) and can tune the band of 12.8 to 13.7GHz. Its gain Kv is varied from $2\pi \cdot 86 \times 10^6$ to $2\pi \cdot 45 \times 10^6$ (rad/sec)/volt over 500MHz tuning band. A conventional active loop filter type is shown in Fig. 5 (a). In a while, the active loop filter configuration proposed in this paper is shown in Fig. 5 (b). The contrived two-stage active loop filter composed of a differential amplifier and lag-lead loop filter is implemented to not only have its natural function but also remove the undesired transient term caused by mismatching of components in a typical loop filter that accommodates two differential outputs of a phase detector[13]. The circuit B is the demensionless factor induced to compensate for the mutual relation between VCO nonlinearity and frequency divider variations. It plays a role to keep uniformly the loop gain and is implemented by a simple voltage divider. In this paper, a new parameter, k'_v, which means the modified gain constant over all tuning band is defined by the following equation.

$$k'_v \equiv \frac{K_v^{(i)}}{N_m^{(i)} B^{(i)}} \ [(rad/s)/v], \quad i = 1, 2, 3 \quad (2)$$

where, the $K_v^{(i)}$, $N_m^{(i)}$ and $B^{(i)}$ are explained in the next paragraph. When it is supposed that 500MHz VCO tuning band is divided into three sub-bands(see Fig. 4), the $K_v^{(i)}$ corresponds to the gain in each sub-band. Similarly, the $N_m^{(i)}$ corresponds to the arithmetic mean of the N range given in each band and the range of N over all tuning band is varied from 161 to 261. First of all, if we

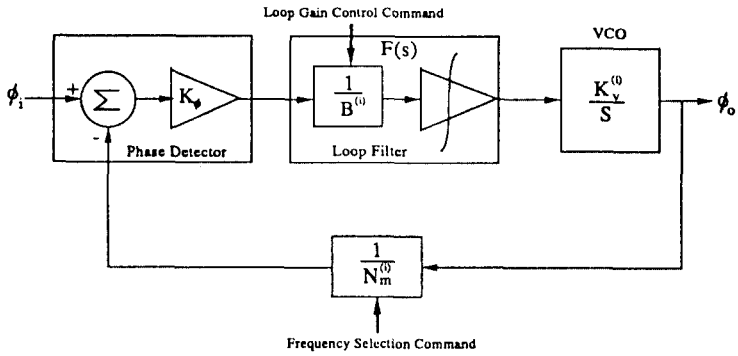


Fig. 3. The block diagram of the PLL feedback control loop

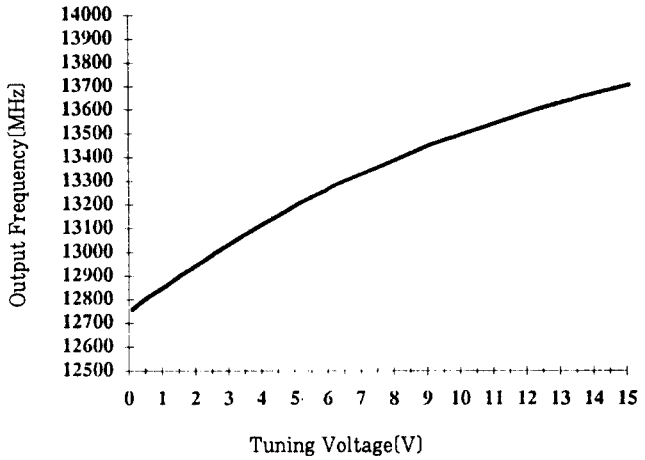
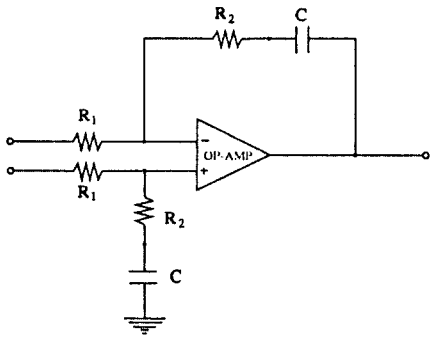
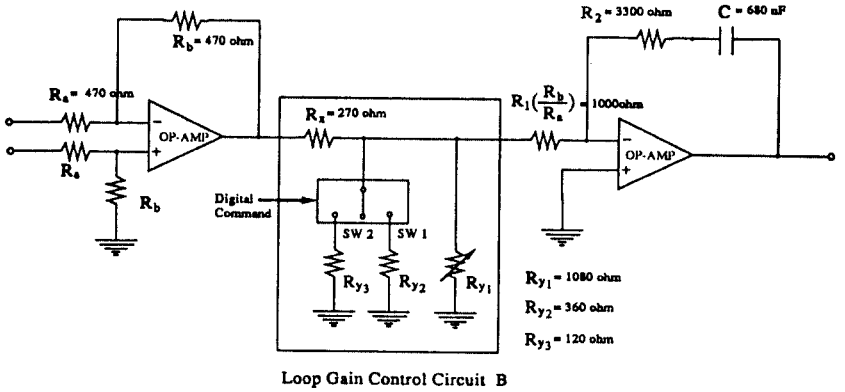


Fig. 4. The I/O transfer characteristic of the microwave VCO



(a) A conventional active loop filter



(b) The proposed active loop filter

Fig. 5. Block diagrams of an active loop filter

set the $B^{(3)}$ in third band to 1.25, k'_v can be determined as 883573 [(rad/s)/v]. After then, the $B^{(1)}$ and $B^{(2)}$ are normalized with respect to this value as shown in Table 1.

Henceforth, the transfer function, F(s), of the active loop filter is given by

$$F(s) = \frac{1}{B^{(i)}} \left(\frac{1 + sT_2}{sT_1} \right) \tag{3}$$

where,

$T_1 = R_1C$, $T_2 = R_2C$

The open loop transfer function of the PLL control system shown in Fig. 3 is expressed by

$$GH(s) = K_\phi \cdot \frac{k_v}{s} \cdot \left(\frac{1 + sT_2}{sT_1} \right). \tag{4}$$

The closed loop transfer function of output phase to input phase in terms of frequency is given as follows.

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{N_m^{(i)}(2\zeta w_n s + w_n^2)}{s^2 + 2\zeta w_n s + w_n^2} \tag{5}$$

and, the natural frequency(w_n) and damping factor(ζ) are given by

$$w_n = \sqrt{\frac{k_v K_\phi}{T_1}}, \qquad \zeta = \frac{w_n T_2}{2} \tag{6}$$

w_n and ζ are usually constrained by the noise performance, stability and settling time requirements of the loop. The ideal time response due to a reference frequency step in an underdamped system is given by the following equation[13].

$$\phi_{error}(t) = \frac{\Delta w}{w_n\sqrt{1-\zeta^2}} \sin(\sqrt{1-\zeta^2}\, w_n t) e^{-\zeta w_n t} \tag{7}$$

The phase error appearing at the VCO output is then N times that at the phase detector input. This is analogous to an output frequency step of N times that at the reference. For this synthesizer design, $w_n = 2\pi \cdot 100$ Krad/sec (f_n = 100 KHz), ζ = 0.707 and t_s = 7.2 sec, settling time, are chosen irrespective of the output frequency or division factor N. Therefore, if C is chosen to be 680 pF, then R_1 = 1000 Ω and R_2 = 3300 Ω can be found from equation (2) and (6).

Table 1. The determination of B with respect to Kv and N_m variations

i	FREQUENCY RANGE[GHz]	$K_v^{(i)}$ [(rad/s)/v]	$N_m^{(i)}$	$B^{(i)}$	SWITCH	
					SW1	SW2
1	13.055~13.205	$2\pi \cdot 86 \cdot 10^6$	176	3.50	OFF	ON
2	13.205~13.455	$2\pi \cdot 62 \cdot 10^6$	221	2.00	ON	OFF
3	13.455~13.555	$2\pi \cdot 45 \cdot 10^6$	256	1.25	OFF	OFF

IV. LOOP STABILITY ANALYSIS

It is very important to guarantee the stabilization of the control loop over the operational band of the frequency synthesizer. There are many different methods of analyzing the stability of feedback control systems[14]. The approach used here is to derive the total open loop transfer function of the control loop and perform the Bode plot analysis. To obtain the exact loop transfer function for the practical design, op-amp finite gain/bandwidth effects, additional poles zeros for reference suppression filtering, the IF filter in the feedback path and other delays in the loop have to be included in equation (2). If these additional effects are neglected during the stability analysis, the consequences can be severe.

With the op-amp(OP-27-GS) response taking into account the effect of the finite voltage gain($A_0 = 1.8 \cdot 10^6$) and gain-bandwidth product($GBW = 8MHz$), the transfer function of the modified active loop filter, $F_o(s)$, becomes as given in the following equation.

$$F_o(s) = \frac{A_o(1+sT_2)}{s^2 T_o(T_1+T_2) + s(T_1+T_2 + T_o + A_o T_1) + 1} \quad (8)$$

where, $T_o = \frac{A_0}{2\pi GBW}$

A_0 : op-amp finite voltage gain

GBW : op-amp gain-bandwidth product

There is a finite propagation delay through the counters which implement the frequency divider, and also there is an inherent sampling delay of one-half the period of the phase comparison frequency. Generally, since the latter is at least an order of magnitude greater than the former, divider delay may be neglected. Because the phase error is encoded using pulse-width modulation, there is an associated output spectrum, with a DC components equal to the duty cycle of the phase error. If the higher frequency components of the output are neglected, the phase detector is modeled with a linear transfer function as follows[15].

$$k_\phi(s) = K_\phi e^{-\frac{s}{2F_{in}}} \quad (8)$$

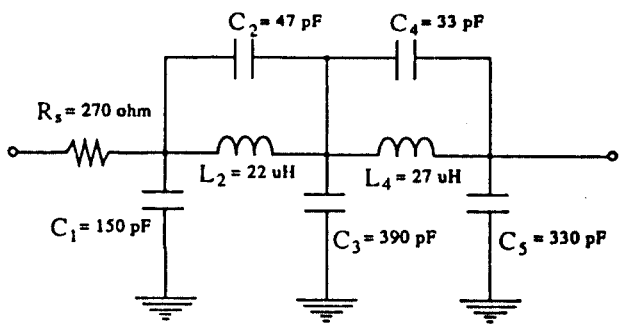


Fig. 6. The block diagram of the reference suppression filter

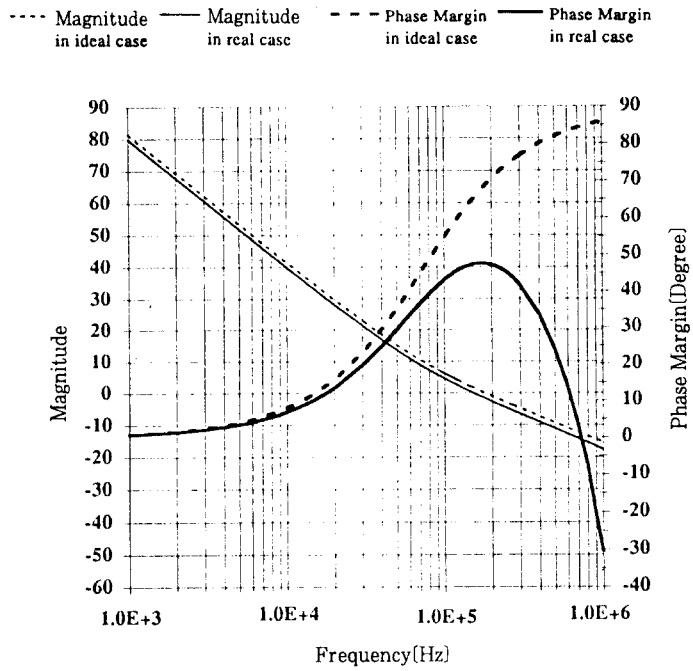


Fig. 7. The frequency response of the open loop transfer function

where,

F_{pd} : the phase detector comparison frequency(5MHz)

The reference suppression filter of the 5th elliptic type as shown in Fig. 6 is used to remove sidebands on the synthesizer output and its voltage transfer function is given

$$f_R(s) = \frac{(L_2C_2s^2+1)(L_2C_2s^2+1)}{As^5+Bs^4+Cs^3+Ds^2+Es+1} \quad (9)$$

where,

$A = R_sL_2L_4(C_1C_2C_4+C_1C_2C_5+C_1C_3C_5+C_1C_4C_5+C_2C_3C_4+C_2C_3C_5+C_2C_4C_5)$

$B = L_2L_4(C_2C_4+C_2C_5+C_3C_4+C_3C_5+C_4C_5)$

$C = R_S(C_1L_2C_2+C_1L_2C_3+C_1L_2C_5+C_1L_4L_4+C_1L_4C_5+C_3L_2C_2+C_3L_4C_4+C_3L_4C_5+C_5L_2C_2+C_5L_4C_4)$

$D = L_2C_2+L_2C_3+L_2C_5+L_4C_4+L_4C_5$

$E = R_S(C_1+C_3+C_5)$

Also, the low pass filter followed by the microwave mixer shown in Fig. 2 degrades the loop stability, but its effect is small enough to be neglected because its cutoff frequency is much greater than the loop bandwidth.

Therefore, the total open loop transfer function, $GH_t(s)$, including all the practical factors mentioned by this time is expressed by

$$GH_i(s) = k_\phi(s) \cdot \frac{k_v}{s} \cdot F_o(s) \cdot f_R(s) \ . \qquad (10)$$

In the real case considering all component effects within the PLL, the frequency response for the open loop transfer function is shown in Fig. 7 in contrast with ideal case. The simulation result of Fig. 7 shows that the unity amplitude frequencies are about 160KHz in the real case and about 180KHz in the ideal case, and the phase margins are about 47° and 69° in two cases, respectively. This result is almost the same with respect to all tuing band. Conclusionly, though the degradation of the phase margin is 22° in the practical design, the phase margin 47° is enough to allow for component tolerances and drift due to aging and temperature, etc.

V. PHASE NOISE ANALYSIS

In the PLL frequency synthesizer, some major noise sources to be considered are the reference phase noise, VCO phase noise, phase detector noise and loop filter noise. These noise sources can be added by the rule of superposition since the loop can be modeled as shown in Fig. 8 and the noise of each block can be estimated. The phase noise of 125MHz digital PLO with the loop bandwidth of 100Hz depends on that of 10MHz reference signal within the loop bandwidth and free running 125MHz VCXO outside it. The specification of 10MHz reference signal used in DAMA-SCPC system is shown in Fig. 1. Similarly, the phase noise of 875 analog PLO with the 20kHz loop bandwidth is affected by those of 125MHz second reference locked to 10MHz first reference and free runnig VCO. In this paper, it is assumed that the estimated phase noise performances at each output of 125MHz digital PLO module and 875 MHz analog PLO module are given as shown in Fig. 9 (a) and (b). The final output phase

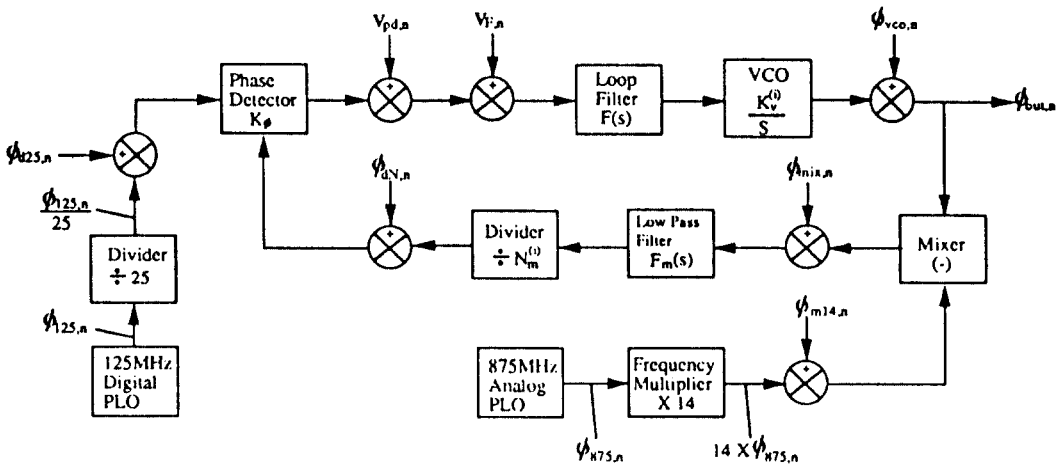
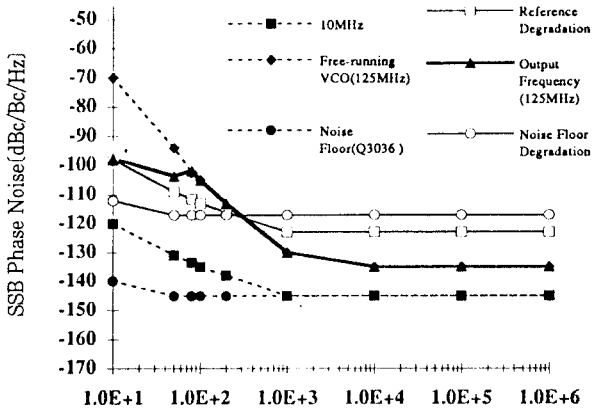
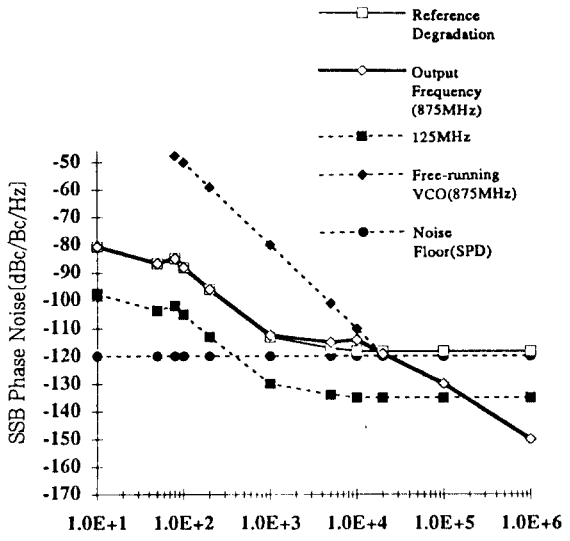


Fig. 8. The modelling diagram for estimating the phase noise of the designed PLL synthesizer.



(a) 125 MHz digital PLO



(b) 875 MHz analog PLO

Fig. 9. The estimated phase noise performance of the first and second module

noise performance can be estimated from the block diagram of Fig. 8. That is, by assuming a locked loop and applying Mason's rule to Fig. 8, the following equation (11) can be derived as

$$\Phi_{out,n}(s) = H'(s)\cdot\Big[\frac{N_m^{(i)}}{25F_m(s)}\cdot\Phi_{125,n}(s) + \frac{N_m^{(i)}}{F_m(s)K_\phi}\cdot\{V_{pd,n}(s)+V_{F,n}(s)\} + 14\cdot\Phi_{875,n}(s) + \Phi_{m14,n}(s) + \Phi_{mix,n}(s) + \frac{N_m^{(i)}}{F_m(s)}\cdot\{\Phi_{d25,n}(s) + \Phi_{dN,n}(s)\}\Big] + \{1-H'(s)\}\cdot\Phi_{vco,n}(s) \quad (11)$$

where,

$$H'(s) = \frac{N_m^{(i)}K_\phi K_v^{(i)}F(s)}{N_m^{(i)}s + K_\phi K_v^{(i)}F(s)F_m(s)}$$

The PLL transfer function $H'(s)$ performs a low-pass-filtering operation on all noise

Table 2. The notation and description for each of the modelling blocks

Component Description		Notation LT-PN(*) [rad]	Notation LT-PNSD(**) [rad²]	Given Performance
125 MHz Digital PLO		$\Phi_{125,n}(s)$	$S_{125,n}(w)$	Refer to Fig. 9(a)
875 MHz Analog PLO		$\Phi_{875,n}(s)$	$S_{875,n}(w)$	Refer to Fig. 9(b)
13 GHz Free Running VCD		$\Phi_{vco,n}(s)$	$S_{vco,n}(w)$	Refer to Fig. 10
Phase Detector		$\frac{V_{pd,n}(s)}{K_\phi}$	$\frac{S_{pd,n}(w)}{K_\phi^2}$	Refer to Q3036 data book[18]
Frequency Divider	Refernece	$\Phi_{d25,n}(s)$	$S_{d25,n}(w)$	
	VCO	$\Phi_{dN,n}(s)$	$S_{dN,n}(w)$	
Loop Filter		$\frac{V_{f,n}(s)}{K_\phi^2}$	$\frac{S_{f,n}(w)}{K_\phi^2}$	Negligible [4,18]
Frequency Multiplier		$\Phi_{m14,n}(s)$	$S_{m14,n}(w)$	Negligible[16]
Microwave Mixer		$\Phi_{mix,n}(s)$	$S_{mix,n}(w)$	Negligible[17]

(*) LT-PN : Laplace transformed phase noise
(**) LT-PNSD : Laplace transformed phase noise spectral density

sources except VCO free running phase noise, and $[1-H'(s)]$ performs a high-pass-filtering operation on VCO noise. The notation and description for each modelling block and added noise source shown in Fig. 8 are in detail summarized in Table 2.

Since all the considered noises are random and uncorrelated, the output noise spectral density can be obtained by summing the respective spectral densities and is represented as the following equation (12) under the assumption that $F_m(s)$ is neglected because its influence is very small within the pass band.

and so $H'(s)$ becomes $H(s)$ given in equation (5).

$$S_{out,n}(w) = |H(w)|^2 \cdot \left\{\left(\frac{N_m^{(i)}}{25}\right)^2 \cdot S_{125,n}(w) + \{N_m^{(i)}\}^2 \cdot \{S_{pd,n}(w) + S_{d25,n}(w) + S_{dN,n}(w) + S_{F,n}(w)\} + 14^2 \cdot S_{875,n}(w) + S_{mix,n}(w) + S_{m14,n}(w)\right] + |1-H(w)|^2 \cdot S_{vco,n}(w) \quad (12)$$

The total output phase noise of the microwave synthesizer for DAMA-SCPC system estimated by means of equation(12) is shown in Fig. 10. The noise floors of the frequency multiplier(X14) and microwave mixer can be neglected[16,17], those of the phase detector and frequency divider are determined by Q3036[18]. Also, the noise floor influenced by the loop filter is a great deal smaller than those of Q3036, so it can be omitted[4,18]. Fig. 10 shows graphically the process to add each noise source in due order.

VI. PERFORMANCE MEASUREMENTS

All, four modules, needed for the

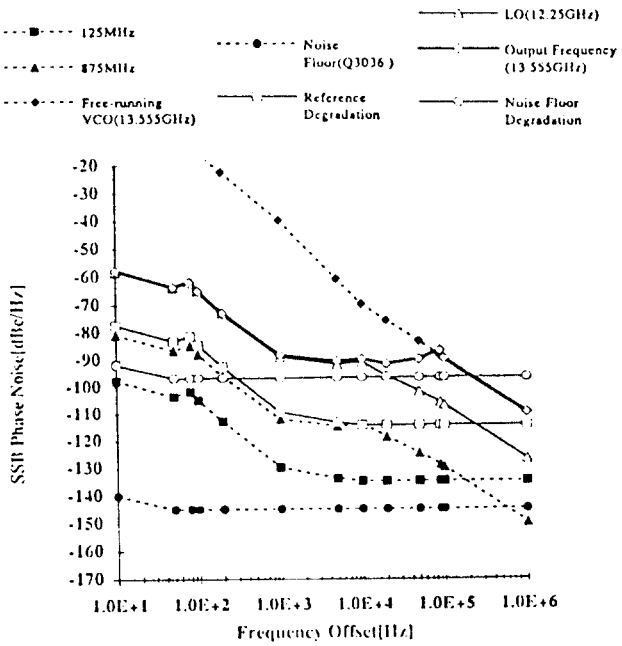


Fig. 10. The estimated total phase noise performance of the microwave synthesizer

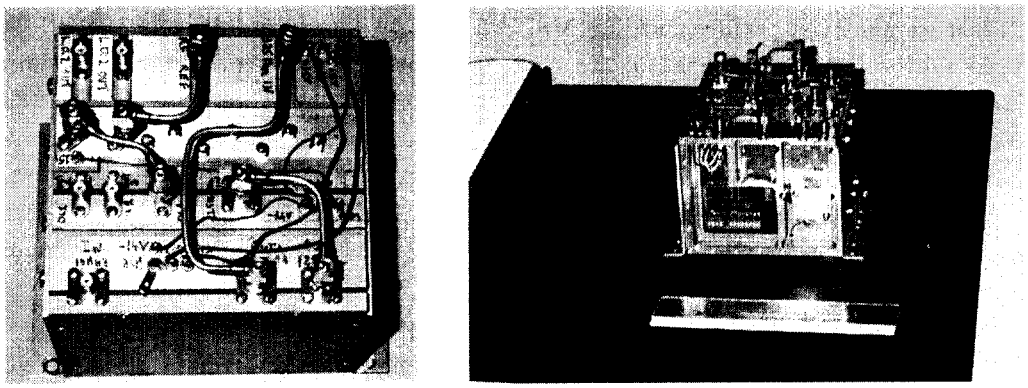


Fig. 11. The actual object of the integrated microwave synthesizer

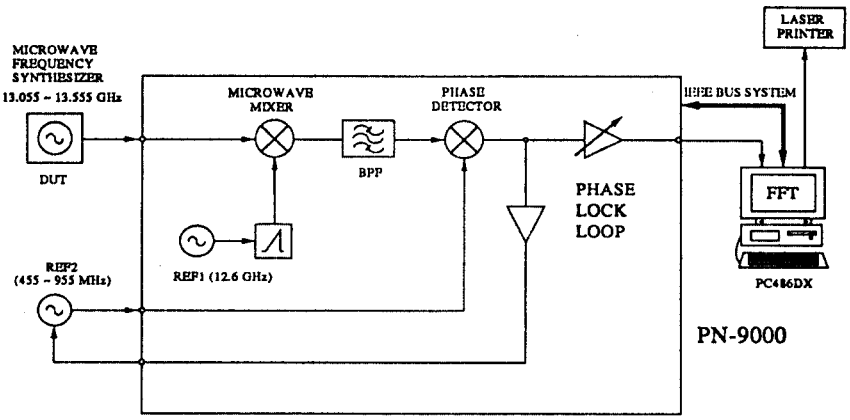
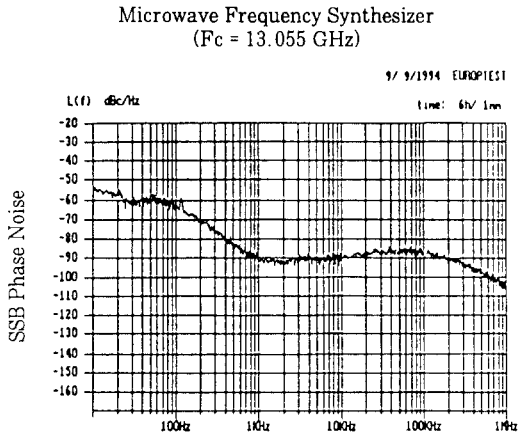


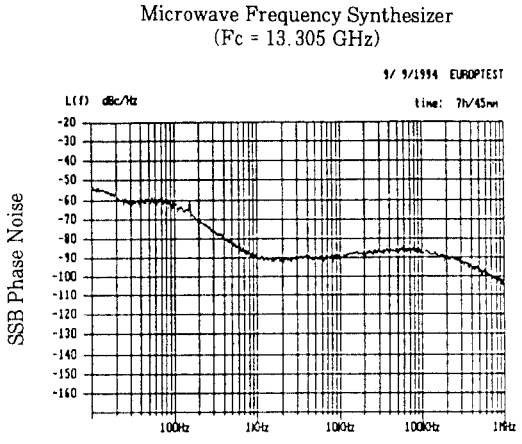
Fig. 12. The experimental set-up for the phase noise measurements

microwave synthesizer are integrated into 10 x 10 x 8.5cm3 package as shown in Fig. 11. It becomes essential that spectral purity parameters such as the phase noise and spurious are measured as a production quality verification to ensure that the performance of this advanced synthesizer isn't degraded due to deficient signal sources. The PN-9000 Automated Phase Noise Measurement System is ideally suited to such requirements because it is a fully integrated system and has beendesigned specifically to facilitate automated phase noise measurements. Hence, the phase noise measurement for the designed synthesizer is performed using the PN-9000 system which can analyze spectrum up to 10 to 40MHz without an external spectrum analyzer. The experimental set-up is shown in Fig. 12. At first, after setting the output signal of the DUT to 13.055GHz, the signal coming from the 10MHz reference unit of DAMA-SCPC system is applied to the external reference input port of the DUT, and also the DC power supplies, +15V & +5V, are applied to the DUT. The signal to be tested from the DUT output is down-converted to the intermediate frequency range of the PN-9000 RF system. The Europtest PN-9200A down-converter as shown in Fig. 12 includes the microwave mixer and the ultra-low-noise synthesized local oscillator(REF 1). And then, REF 2, a standard synthesizer, is locked by the PN-9000 through its FM DC input, and the FFT(fast fourier transform) spectral analysis and data processing for its output are made with the help of the 486DX PC computer interfaced through an IEEE Bus System. With minor change, the phase noise for every signal to be tested from the DUT can be precisely measured with the same set-up given in Fig. 12.

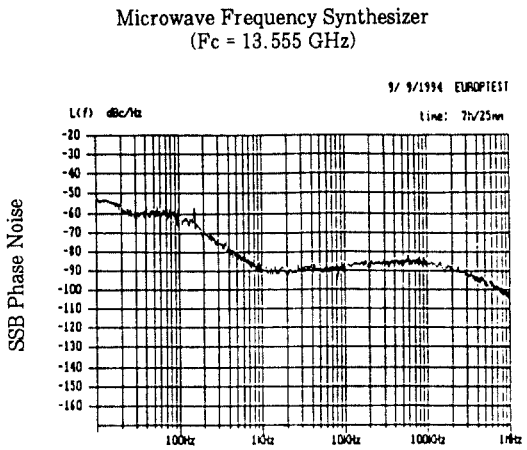
The SSB phase noise performance measured



(a) fc = 13.055 GHz



(b) fc = 13.305 GHz



(c) fc = 13.555 GHz

Fig. 13. The phase noise performance at three output frequencies

Table 3. The integrated phase noise up to 30 KHz offset

Output Frequency [GHz]	Phase Noise Density		Integrated Phase Noise[rms degree]		
	Offset [KHz]	Performance [dBc/Hz]	10Hz~ 30KHz	30Hz~ 30KHz	300Hz~ 30KHz
13.055	1	-91.3	1.04	0.91	0.53
	10	-89.9			
	100	-88.4			
13.305	1	-90.4	1.05	0.93	0.56
	10	-88.7			
	100	-87.3			
13.555	1	-90.1	1.09	0.96	0.58
	10	-88.1			
	100	-87.0			

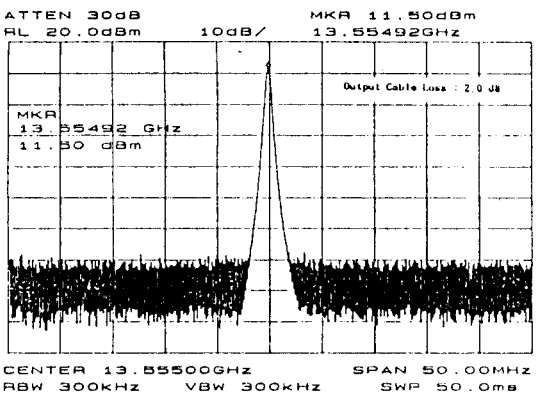


Fig. 14. The output spectrum of the designed microwave synthesizer

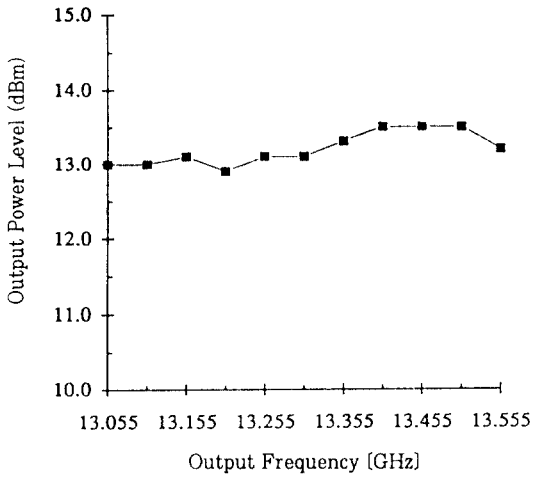


Fig. 15. The output power level and its flatness

at three output carrier frequencies(fc=13.055, 13.305, 13.555GHz) are shown in Fig. 13. Comparing the experimental result of Fig. 13 (c) with the estimated result (see Fig. 10), it can be known that the phase noise difference is a maximum 2dB over the full range of 1MHz offset. From all performance curves of Fig. 13, it can be also shown that the measured performance variations over all tuning band are within a maximum 1dB.

Since DAMA-SCPC system services telephone and data via Korea Satellite have low transmmision rate(32Kbps), it is important, above all, to have low phase noise by up to 30KHz offset to prevent the system performance from being degraded. Referring to Fig. 13, each integrated phase noise amount can be calculated and those values are listed in Table 3 together with the SSB phase noise densities. The initial offst of integration is determined by the loop bandwidth of a coherent demodulator in a digital communication system, and is typically about 0.001 to 0.01 times of the symbol rate. In the case of DAMA-SCPC system, it is about 30Hz, and the maximum integrated phase noise is 0.96rms degree at fc=13.555GHz. An example of the measured output spectrum is shown in Fig. 14, and the output levels in the full tuning band are also measured and those results exhibit that the maximum ripple is less than 1dB(p-p) as shown in Fig. 15.

VII. CONCLUSION

The microwave frequency synthesizer with low phase noise characteristic has been successfully developed for DAMA-SCPC system which shall provide telephone service and data service with low transmission rate

through Korea Satellite. The design approach to consider the practical effect of all components included within circuits was proper for estimating accurately the loop stability and the phase noise density, and the PLL's bandwidths over the full tuning band were uniformly kept by the devised loop gain control circuit. The measured phase noise performance of the synthesizer which has been composed of three PLLs met the required specification over all region. Especially, from the output result of 13.555GHz, the SSB phase noise of the designed synthesizer was as low as -88dBc/Hz at 30KHz offset, and the integrated phase noise over 30Hz to 30KHz offset was 0.96rms degrees. The nominal output power of the synthesizer was 13dBm, and its flatness was less than 1dB(p-p) in the full tuning band. Since this microwave synthesizer has low phase noise characteristic and considerably compact, it can be utilized as microwave local oscilators in satellite communication system and its technology will contribute to the development of new milimeter-wave synthesizers in the future.

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