論文 98-23-3-29

An Evaluation Of Failure Rate Of Printed Board Assemblies To Enhance An Operability Of Telecommunication System

Choong-Reol Yang* *Regular Members*

통신시스템의 운용 능률을 향상시키기 위한 단위 PBA 고장율 평가

正會員 양 충 렬*

ABSTRACT

We, in this paper, summerize the work in the field of assessing the reliability of a set of printed board assemblies of a switching system, applying the method of the high temperature accelerated life test. We have conducted a test with 30 samples under the test conditions obtained by applying the Arrhenius model with the calculated accelerated factors using the complexity factors. Test result are analyzed applying the Weibull-log linear model. The analysis show that the design characteristics are adequate to satisfy the requirement of reliability. This results will be used as basic data to improve efficiency of operating of telecommunication systems and reliability of manufacturing of board assemblies.

요 약

본 논문은 고온도 가속 수명시험 방법을 적용하여 통신 시스템에 사용된 PBA의 신뢰성 평가에 관한 연구이다. 복잡성 인자를 이용하여 계산된 가속 인자들을 아레니우스 모델에 얻은 시험조건에서 30개의 샘플로 시험을 실시하였다. 시험결과는 와이블 로그 선형 모델을 적용하여 해석하였으며 해석 결과는 설계 특성이 신뢰도 필요조건을 만족하는 것으로 나타났다. 이러한 결과는 보드 조립체의 제조 신뢰성 및 통신 시스템의 운용 능률을 향상시키기 위한 기초 자료로 사용된다.

*충남대학교 전자공학과
論文番號:97240-0721
接受日字:1997年 7月 21日

Ⅰ. Introduction

The life time of a switching system is longer than a ten year, so the prediction of reliability of a system is important. A switching system is consisted of many printed board assemblies (PBA) and each PBA contains many components of different kinds depending on applications. Thus, a method to estimate failure rate at PBA level, which can be used to predict over-all reliability of a switching system, is needed.

Under the more or less controlled operational conditions, the changes of thermal conditions may be regard as the main stress which cause failures of PBAs, because components of a PBA are mostly integrated circuits.

In practical problems one strives for the accurate system's reliability, while keeping testing effort at an acceptable level. It is widely accepted that high temperature accelerated life test (ALT) is the most feasible approach to assess the reliability of a system whose main failures are due to thermal effects[1], [2], [3], [4].

The present work is concerned with the high temperature accelerated life test (ALT) at a PBA level. In applying the ALT, it is need to determine acceleration factor which can be used to estimate test temperature, sample sizes and test duration. There are many studies for the calculations of accelerations factor for a PBA [1], [5].

In [1], L.Hart suggest the method of calculating the acceleration factor of a PBA by giving the complexity of components as weight to each acceleration factor of components. There is an alternative study for calculating an acceleration factor. In [5], Moura considered a method to estimate the acceleration factor for sub-assemblies. The method use a weighted average of the acceleration factor of each component in a subassembly to estimate the acceleration factor of a subassembly, so each weight contributes to the total failure rate of a subassembly. Because PBAs under the considerations throught this paper are composed of many ASIC components which are different in complexity, we follow the method of L.Hart for the estimation of acceleration factor of two sample PBAs.

In section 2, we redescribe the method of calculating accelerated factor due to L.Hart for the completeness. Acceleration factors for the two samples of PBA are approximately 100 and 90, respectively. These acceleration factors for each sample PBA are used to estimate the minimum sample size as 30, and test duration as 1,000 hours under the test temperature 125℃.

In section 3, we describe the detailed ALT procedures performed on two sample PBA and the failure data, and analyze them using the Weibull log-linear model.

Ⅱ. Acceleration Model

2.1 Assumptions

Three assumptions in [1].

- Passive components contributes a negligible amount to the failure rate od a properly designed and built assmebly.
- The effect of device complexity factor on failure rate is described by the complexity factor from MIL-HDBK-217D.
- Failure rates of the semiconductor devices in the assembly are constant.

2.2 Model description

Notations

λ: failure rate
E_a: activation energy(eV)
T: Absolute temperature in Kelvin(K)
k: Boltzmann's constant(8.617×10^{-5} eV/K)
T_J: Junction temperature(℃)
T_A: Ambient temperature(℃)
θ_{JA}: Thermal resistance to a ambient temperature ℃/W
P_d: Consumed power(W).
λ_{TJ}: Failure rate of components at temperature T_J

n: A total number of components of each type in a PBA

N: Number of active elements of components in a PBA

C_i: Complexity factor of a component of type i

$C_{n,i}$: Normalized complexity of component of type i.

f_i: Number of used times each component of type i in the PBA.

A_{Fi}: Acceleration factor of component i.

In this section we re-describe the method of calculating an acceleration factor for a PBA following[1]. A failure rate model using temperature as the stress parameter can be expressed as the Arrhenius equation

$$\lambda = A \cdot \exp^{\frac{E_a}{KT}}. \tag{1}$$

Since the junction temperature is expressed

$$J = T_A + \theta_{JA} \cdot P_d, \tag{2}$$

if components consume low power during operation, then there is no difference between T_J and T_A. We assume that $T_J = T_A$.

2.3 Calculation of weights of components in terms of their complexity

Since components of a PBA have different thermal nature, to calculate the acceleration factor for a PBA, we give weights to each components of a PBA by the following formula

$$C_{n,i} = \frac{C_i}{\sum_{j=1}^{N} f_i C_i}. \tag{3}$$

The normalized complexity is used to weight the acceleration factor for each component in the PBA during the accelerated test. We define the weight of each component in terms of its complexity, which will be used to calculate the acceleration factor for a PBA as follows

$$C_{w,j} = f_i \cdot C_{n,j},\ j = 1, \cdots, n,\ (\textit{no summation}). \tag{4}$$

Here, $C_{w,j}$ represents the cumulative complexity contribution to the PBA.

2.4 Acceleration factor of a PBA

An acceleration factor is defined as the ratio of the duration needed to obtain identical failure rates from two identical samples under two different sets of stress conditions with identical failure shapes and mechanisms. The acceleration factor for components may be obtained using the activation energy and the Arrhenius equation. In the case that the junction temperature changes from T_{J1} to T_{J2}, the accelerated factor of component of type i becomes

$$A_{F,i} = \frac{\lambda_{T2,i}}{\lambda_{T2,i}} = \exp\left[\frac{E_{a,i}}{K}\left(\frac{1}{T_{j2}} - \frac{1}{T_{j1}}\right)\right]. \tag{5}$$

The accelerated factor A_i of component of type i represents the contribution of each component type to an acceleration factor for a PBA.

Now, we define a acceleration factor AF for a PBA as follows:

$$A_F = \sum_{j=1}^{n} C_{w,j} \cdot A_{F,i} \tag{6}$$

where $C_{w,j}$ is the contribution of each component type j to an acceleration factor for a PBA.

For the same relation holds at a PBA level as in (5), so if a test failure rate is λ_{T1}, then the operational failure rate, λ_{T2}, may be obtained as λ_{T1}/A_F. In other words, the failure rate at the operational temperature may be calculated from the failure rate data at test temperature.

2.5 Acceleration factors

The acceleration factors for the components are calculated from the activation energies in column 4 in 〈Table 1〉 and the Arrhenius relation. Each sample PBA contains the components shown in 〈Table 1〉 and 〈Table 2〉, classified according to their types.

The types of active elements in each 〈Table 1〉 and 〈Table 2〉 are classified into the four classes, LSI containg micro-processor, TTL, ASIC containg FIGA and EPLD, and memory as simple as possible. We regard one NAND gate as one gate in logic gates and one bit of SRAM as one gate, one bit of DRAM as one half gate, four bit in ROM as one gate in memories. In FIFO, in particular, we calculate the number of active elements of memory by applying the calculation method of memory, and that of logic gate by applying the calculation method of logic. The number of active elements are obtained applying the values of MIL-HDBK-217D.

Table 1. Compexity data for a type 1 PBA

I	N	C	E_a	f	C_n	C_w	A_{Fi}
1	112,640	9.80	0.40	2	0.77	1.54	11.1
2	986	1.53	0.96	24	0.12	2.88	326.0
3	76,000	28.90	0.45	11	2.28	25.08	15.0
4	4,275,984	38.80	0.80	23	3.06	70.38	123.0

Table 2. Compexity data for a type 2 PBA

I	N	C	E_a	f	C_n	C_w	A_{Fi}
1	2,000	9.80	0.40	2	8.60	17.20	124.0
2	264	1.53	0.96	24	1.34	32.16	326.0
3	528	1.89	0.45	4	1.66	6.46	15.1
4	512,000	25.00	0.80	2	21.95	43.90	124.0

2.6 Calculations of the acceleration factor of PBAs

The Arrhenius model equation (5) is used for calculating the acceleration factors due to temperature, for each component od a PBA.

In 〈Table 1〉 and 〈Table 2〉, C is the parameter of complexity of each component adapted in MLD-HDBK-217D standards.

The normalized complexity C_n of each component is calculated by (4) with data of the complexity of each component in column 6 in the Table 1 and Table 2, respectively.

The weight of complexity C_w are calculated by (3) as shown in column 7, in each Table. Using (6), we have the acceleration factor for a PBA of type 1,

$$A_{F1} = 0.17 + 9.38 + 3.75 + 86.1 = 100. \quad (7)$$

and for a PBA of type 2,

$$A_{F2} = 1.1 + 15.7 + 15.1 + 54.4 = 90. \quad (8)$$

Ⅲ. Actual Experiments

3.1 Accelerated Life Test

The sample boards are chosen at the end of software test from the system in the laboratory. An average activation energy of a PBA is assumed to be 0.75eV following the general agreements. The acceleration factors of each sample PBA are 100 and 90 as in (7) and (8).

Since the A_F is known, we performed the highest temperature ALT based on constant-stress. Since passive components have a little effects on failures due to a thermal effect and most of the components are of IC type, we neglect the effects by passive components. To maximize the efficiency in the test, we choose the possible highest test temperature, 125C, which was weidly accepted as an appropriate test temperature (see [1].)

Test time is expressed as lifetime divided by ambient temperature. The reliability requirement of a switching system is 5 failures in 10 years. To meet this requirement, applying the acceleration factor obtained in (7) and (8), two kinds of PBAs are stressed under the temperature 125℃ for 400 hours. So one hour on test at 125C is roughly equivalent to 100 hours in a specified worst-case operating environment, that is, 55℃.

The life-stress relation follows a Weibull-Arrhenius model. The A_F between 40℃ and 125℃ is a known constant. The sample size for the test is chosen as 30 based on Chi-square distribution

3.2 Failure data

The PBAs being stressed in the 125℃ oven were removed at the 12−, 24−, 48−, 72−, 96−, 200−, 300−, 400-hour points and tested by test jigs and in the host switching system. In tests, the first failures are experienced at VLSI devices, gate arrays and power modules near 12-hour test-point caused by the manufactoting errors. Successive failures are occurred in sockets, and capacitors by short of components, demage of ESD, and disconnected patterns at successive test point. In Table 3, we summarize the amount of failures.

<Table 3>. Failure data

Time / PBA	12	24	48	72	96	200	400
Type 1	1	1	0	0	2	1	1
Type 2	2	1	1	0	1	2	2

3.3 Analysis of failure data

A Weibull distribution is assumed for the reliability distribution of a constant stress. We use the Weibull log-linear model to analyze the failure data. Assessed failure rate obtained from the ALT for all PBAs by applying Weibull distribution model is shown in 〈Table 4〉 and their log-linear graphs are shown in (Figure 1), and (Figure 2). The figures shows that the Weibull distribution assumption is adequate.

<Table 4>. Failure rates of each sample PBA

Test Samples	Quantities	Failure Rate
Type 1	15	9×10^{-6}
Type 2	15	6×10^{-6}

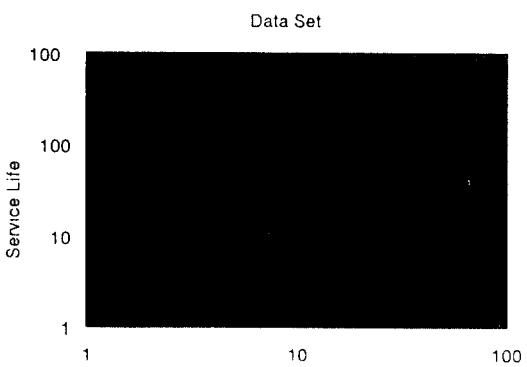

Figure 1. Log-Log graph of failure data set 1.

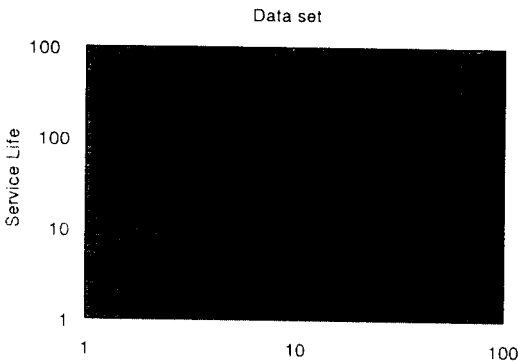

Figure 2. Log-Log graph of failure data set 2.

Ⅳ. Conclusions

In real applications of a switching system the remeady of failures of hardware is performed in a unit of PBA, and so it is important to assess the failure rate of a PBA. Under the controlled operational conditions the failure of PBA is seemed to occur mainly by the changes of temperature. High usage of devices adopting the recent technologies, for example, micro-processor, ASIC, TTL, etc, to design a PBA lead us to consider the complexity as the most important attributes of failures of PBA.

The acceleration factors for PBA is obtained by applying the method which use the complexity factor to estimate the acceleration factor for a PBA. We apply them to conduct the high temperature ALT to PBA to assess the failure rate of PBA. According to test results, high failure rates was recorded at the component having big complexity. The two sample boards are the most complex board and they constitute 80% in the control subsystem of the switching system under study. While there are failures during the test, through the understanding of the failure

mechanism by changes of temperature, the adequacy of design of PBAs are sufficiently guaranteed.

References

1. L. Hart, "Reliability of an Electronic Assembly; A Case History", *IEEE Trans. on Reliability*, Vol. R-36, No. 4, pp. 385~389, 1987.
2. D. Holcomb, J. C. North, "An Infant Mortality and long-term failure rate Model for Electronic Equipment", *AT&T Technical Journal*, Vol. 64, No. 1, pp. 15~31, 1985.
3. D. M. Barry, D. C. Vontas, "Statistical Reliability and Failure Arrhenius Models for Temperature Stressed Transistor", *Rel. in Electrical and Electronic Components and Systems*, pp. 239~242, 1982.
4. M. Stitch, et al, "Micro-circuit Accelerated Testing using High Temperature Operating Tests", *IEEE, Trans.on Reliability*, Vol. R-24, No. 4, 1975.
5. E. C. Moura, "A Method to Estimate the Acceleration Factor for Subassemblies", *IEEE, Trans.on Reliability*, Vol. 41, No. 3, pp. 396~399, 1992.

양 충 렬(Choong-Reol Yang) 정회원

1983년 : 건국대학교 전자공학과 (학사)

1986년 7월~1992년 6월 : (주)현대정공 기술연구소

1989년 : 미국 제너럴다이내믹스(GDLS)사 파견 연구원

1992년 6월~1997년 현재 : ETRI 광교환 연구실 선임연구원

1997년 12월 : 충남대학교 공대 전자공학과(석사수료)

※관심분야 : 통신 및 제어, 신호처리