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광대역 CDMA WLL 시스템을 위한 변조기 채널 카드 및 VLSI 칩 설계 및 구현

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Design and Implementation of Modulator Channel Card and VLSI Chip for a Wideband CDMA Wireless Local Loop System

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요 약

본 논문은 Direct Sequence Code Division Multiple Access (DS-CDMA) Wireless Local Loop (WLL) 시스템의 Radio Transceiver Unit (RTU)를 위한 변조기 채널 카드와 변조기 VLSI 칩의 설계 및 구현에 대해서 서술했다. 변조기 채널 카드는 ASIC, FPGA 그리고 DSP를 이용해서 구현하였다. 구현된 변조기 ASIC칩은 ETRI가 제안한 Common Air Interface (CAI) 규격을 따랐고, 동작주파수는 32MHz, 회로의 크기는 40,000 게이트이다. 그리고 0.6 μm CMOS 공정으로 제작되었다. 본 변조기 ASIC 칩은 4개의 I,Q 채널을 처리할 수 있는 구조로 되어 있고 각 채널은 콘벌루션널 코딩, 블록 인터리빙, 스크램블링, 왈쉬 카버링, Pseudo Noise (PN) 확산 그리고 기저대역 필터링 기능 등을 포함한다. 변조기 채널 카드는 WLL 시스템 내 RTU의 서브 유니트의 하나이며 구현된 변조기 ASIC 및 채널 카드는 실제 WLL 시스템에 실장되어 그 성능 및 기능 요구사항을 만족함을 확인할 수 있었다.

ABSTRACT

In this paper, we present the Modulator Channel Card and VLSI chip for the Radio Transceiver Unit (RTU) of direct sequence code division multiple access (DS-CDMA) Wireless Local Loop (WLL) System. The Modulator Channel Card is designed and implemented using ASIC's, FPGA's and DSP's. The ASIC, compliance with Common Air Interface specification proposed by ETRI, has 40K gates which is designed to operate at 32MHz, and is fabricated using 0.6 μm CMOS process. The ASIC carries out four I- or Q- phase data channel signal processing at a time, where each data channel processing consists of channel coding, block interleaving, scrambling, Walsh modulation, Pseudo-Noise (PN) spreading, and baseband filtering. The Modulator Channel Card has been integrated as a part of RTU of WLL system and is confirmed that it meets all functional and performance requirements.

I. Introduction

Future wireless systems will provide a large number of services to their customers, and their data rates will be increased up to 2Mbps. With high capacity and other advantage such as simple cell planning, wideband Code Division Multiple Access (CDMA) system has been considered as a potential candidate for future wireless system in several research projects all over the world.

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An application of wideband CDMA system is CDMA based Wireless Local Loop (WLL) system that has been developed extensively in several countries. In Korea, the draft version of wideband CDMA Common Air Interface (CAI) for WLL system is submitted to Korean Telecommunication Technology Association (KTTA) for standardization[1]. It operates at 2.3~2.33 GHz for the reverse link and at 2.37~2.40GHz for the forward link, and supports several bandwidths of 3.5, 5, 10, 10.5, and 15MHz.

The wideband CDMA WLL system developed by ETRI mainly comprises Radio Subscriber Unit (RSU), Radio Transceiver Unit (RTU), and Transcoding & Network Unit (TNU). Figure 1 shows the system configuration of the WLL System. The WLL subscribers are connected to RSU and the WLL system itself is connected to PSTN by subscriber line interfaces at TNU. Also test phones are connected to TNU for the test purpose.

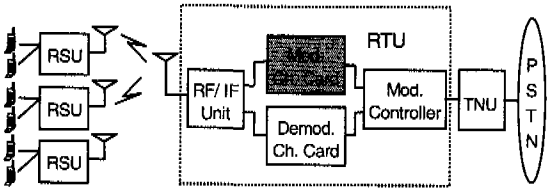

Fig. 1. The system configuration of wideband CDMA WLL system

The Modulator Channel Card carries out CDMA baseband signal processing for the forward link of the WLL system. In the WLL system, there are several physical channels in the forward link: a pilot channel, a sync channel, a paging channel, and a number of forward traffic channels. The Modulator Channel Card is designed to process any forward link physical channel with a single hardware. The implemented Modulator Channel Card meets functional and performance requirements in itself, and also operates well when it is integrated to the WLL system.

In this paper, the system requirement and architecture of Modulator Channel Card are described in section II. The more detailed functions of the Modulator Channel Card and algorithms used in the ASIC chip design are summarized in section III. Section IV describes the timing of the major signals on the forward link. The implementation of the Modulator Channel Card is described in section V.

II. Architecture

The Modulator Channel Card is designed to meet the following functional and performance requirements.

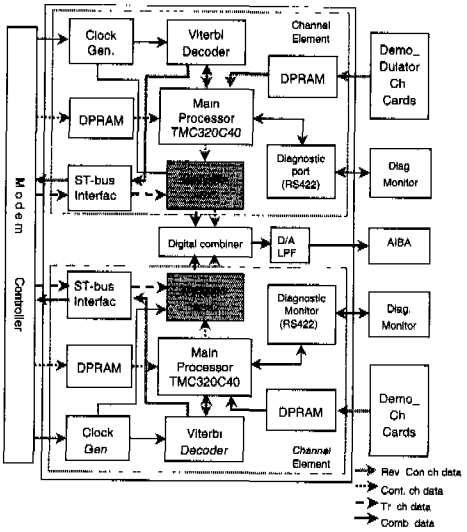

Fig. 2 Functional block diagram of the modulator channel card

- DS-CDMA baseband signal processing
- Radio resource management
- Power control
- E1/T1 interface to TNU
- Viterbi decoding
- Eight I- or Q- phase data channels processing per one modulator card
- 4.096MHz or 8.196 MHz PN chip rate

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- Max. 144Kbps Data transmission rate

For the forward link, the Modulator Channel Card has TMS320C40 DSP's, ST-bus interface, modulator ASIC's, and DPRAM's for Modem Controller interface. For the reverse link, it has two Viterbi decoders, and DPRAM's for the Demodulator Channel Card interface. It has RS422 port for diagnosis and RS232C port for debugging.Functional block diagram of the Modulator Channel Card is shown in Figure 2.

Ⅲ. Detailed functions and Algorithm

1. Operations of modulator channel card

The functions of the Modulator Channel Card of the WLL system are the modulation for the forward link and Viterbi decoding for the reverse link. For the forward link, the Modulator Channel Card modulates channel data, converts them to analog signals at digital to analog (D/A) conversion module, and sends them to Analog Interface Board Assembly (AIBA). The analog signal received from the Modulator Channel Card is up-converted to Intermediate Frequency (IF) at the AIBA, and is send to RF module. For the reverse link, the Modulator Channel Card receives channel data from the Demodulator Channel Card, decodes them by Viterbi decoder, and sends them to Modem Controller through DPRAM.

As the Modulator Channel Card determines the personality (operating channel type and necessary parameters) of each channel element by loading the setup commands to the specific control registers of the modulator ASIC chips, it can operate as any of traffic channel data, signaling channel data and control channel data with single hardware. Therefore all the Modulator Channel Cards used in the RTU are of a kind. The data rates implemented in the Modulator Channel Card are from 32 to 144kbps for traffic channel and 8kbps for control and signaling channel.

When operating for the forward traffic channel data, the Modulator Channel Card receives the data from Modem Controller through ST-bus interface and processes them at the modulator ASIC rather than at DSP. As the DSP load by the traffic channel data is not significant in this structure, the channel capacity of the Modulator Channel Card can be expanded relatively easily, just by exchanging the ASIC chips. The modulated data is combined with control channel data, and sent to the AIBA after D/A conversion. When operating as the control channel such as pilot/sync and paging channel, the Modulator Channel Card manages the control channel based on the message received from the Modem Controller through DPRAM. In the case of access channel data, the data received from the Demodulator Channel Card is decoded by Viterbi decoder chip and the decoded data is sent to the Modem Controller through DPRAM. In the case of control and signaling channel data for the reverse link, DPRAM is used in the data transmissions between the Modulator Channel Card and the Modem Controller, while ST-bus interface is used for forward traffic channel data.

A Modulator Channel Card is made up of two identical modulation modules which operate independently. Here, the modulation module means the basic unit that processes all the functions of Modulator Channel Card, and is designed to process two forward link physical channels at a time. Therefore, a Modulator Channel Card can handle four forward link physical channels at a time, and it has two Viterbi decoders for the reverse link channels.

2. Viterbi decoder

To balance the processing load between the Demodulator Channel Card and the Modulator Channel Card, the Modulator Channel Card has the Viterbi decoding function for the reverse link.

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Moreover, it is advantageous in the hardware complexity because only the Modulator Channel Card is needed to have the ST-bus interface then. The Modulator Channel Card receives the demodulated data from the Demodulator Channel Card through DPRAM. The traffic channel data is decoded by commercial Viterbi decoder chip manufactured by Qualcomm and the decoded data is sent to the Modem Controller through ST-bus interface. The signaling and access channel data are decoded at the DSP by software.

3. ST-bus interface

Each data for the forward link channel is sent from TNU to the Modem Controller through E1 link. And the Modulator Channel Card receives the channel data from the Modem Controller through ST-bus interface. The timing diagram of data latch from ST-bus interface is shown in Figure 3. Modulator ASIC latches 8 bits with 8 kHz for 64 kbps traffic data. If data rate is as high as that of the traffic service, the data is sent from ST-bus to ASIC directly, bypassing the DSP to reduce the DSP load.

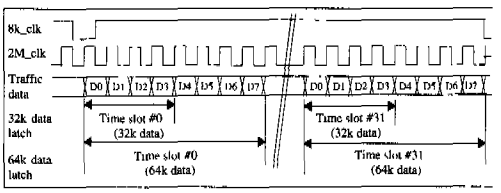

Fig. 3 Traffic data latch timing from trunk

4. Modulator ASIC

Here, modulation of control or traffic channel data includes encoding, block interleaving, scrambling, Walsh modulation, spreading, and filtering. Each of these functions is discussed below. The functional block diagram of modulator ASIC[2] is shown in Figure 4.

1) Channel coding and modulation part

The data to be transmitted on the forward link channel is convolutional encoded at the modulator prior to interleaving. Every 20ms (a frame), the DSP puts data into the input buffer of convolutional encoder whose constraint length is k = 7 and rate is 1/2. The convolutional encoder is generally used in communication systems with its simple structure and easy to design, but its performance is sensitive to bursty errors. Therefore block interleaving is used to avoid burst errors by randomizing burst errors. The coded symbols are written to the block interleaver memory by rows and the interleaver contents are then read out by columns. The orders of columns to read out change depending on the data rate and the channel type.

For the traffic channel data symbols, data scrambling is applied to the output of the interleaver, which is to secure the privacy of the call. Data scrambling is exclusive OR operation of data symbol and scrambling code which is pseudo-random sequences produced by a 16-bit PN sequence generator operating with 32KHz. As the rate of scrambled code is fixed to 32KHz, it is adjusted to the various data rates of traffic channel by decimation. The scrambling code assigned to each traffic channel is unique with period of even second which is selected from the

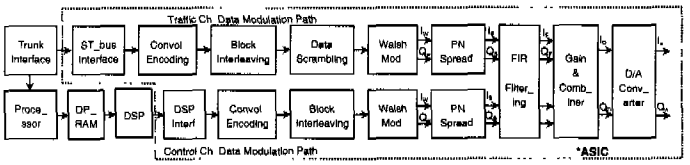

Fig. 4 Block diagram of modulator ASIC

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whole sequence with the period of 2^{16} - 1 chips. The scrambled data is then separated into I- and Q- phase data stream at serial/parallel converter by QPSK spreading.

To identify each user, the Walsh code is used. The Walsh modulator multiplies the interleaved symbol stream by an orthogonal function, the Walsh code. Sometimes, the Walsh modulation is called Walsh Covering. The Walsh code is a row vector of Hadamard matrix which is extended from basis code matrix as shown in Equation (1).

$$H(2^N) = \begin{pmatrix} H(2^{N-1}) & H(2^{N-1}) \\ H(2^{N-1}) & \overline{H}(2^{N-1}) \end{pmatrix} \quad (1)$$

After the Walsh modulation, the I- and Q-phase signals are spread by respective PN sequences. The I- and Q- channel PN sequences are generated by respective 32-bit PN generators each of which has different generator polynomial. Each PN generator is preset to a specific state, and commences a cycle through a full 2^{32} states. Here PN sequence lengths are normally 2^{n-1} where n is the number of shift registers in the PN generator. Its implementation method is basically the same as that of scrambling PN code generator used in scrambler, but in this case 2^{32} - 1 number of PN's are generated. When the system uses shortened PN code, the PN generator is initialized every 20 ms and thus only 81920 numbers of PN's are used.

2) Baseband FIR filter

After the PN spreading, the baseband filtering limits the bandwidth of the transmitted signals, as required by CAI to suppress the interference to the adjacent CDMA radio channels. Four 48-tap FIR filters are required, two of which are for the baseband filtering of I-phase data streams and the other two are for the Q-phase data streams. These filters have symmetric coefficients, and its sampling frequency are four times of the frequency of the data stream.

In the conventional filter design, multiplier and adder cell (MAC) for 48 taps filter takes most of the volume and makes the hardware very large. As shown in figure 5, we propose a new FIR filter structure that four I- or Q- phase data channels share the coefficients and adders to reduce the design area. As the coefficients of the four FIR filters are same, instead of using four identical FIR filters, only a FIR filter is used in the ASIC design with increasing the operation speed four times. The multiplication of coefficients by zeros which is inserted by a factor-of-4 interpolation always result in zeros. Only 12 coefficients are meaningful in the multiplication at a time and there are four sets of these 12 coefficients. Therefore in the ASIC, the FIR filter is designed to operate only for these 12 coefficients at a time and repeat the multiplication four times for each coefficient set every data input. While its operation is absolutely the same as that of the 48 tap interpolation FIR filter, the hardware complexity and size are reduced drastically.

Filter coefficients are represented by 13 bits and the MSB bit indicates the sign; '0' for positive values and '1' for negative values. In 2's complement representation, some coefficients with smaller absolute value can be represented by less than 13 bits as they have some repeated 0's or 1's on the MSB side in 13 bit representation. For example,

```
coeff_0  :  b"1111110011101 "=>b"110011101 " (4bit truncation)
coeff_4  :  b"0000001010100 "=> b"0001010100 "(3bit truncation)
coeff_45 :  b"1111110111111 " => b"110111111 " (4bit truncation)
```

These repeated bits can be truncated leaving only one of them with no loss of information. To make the bit truncation effective, coefficients of the same bit length are arranged to be added together (for example, coeff_0 + coeff_44).

In the proposed filter architecture, the size of

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implemented hardware and the number of adder could be reduced less than one half.

3) Gain Control Block and Data Combiner

The DSP controls the transmission output of modulator. 12-bit output of FIR filter is multiplied by gain which is represented by 8 bits. The operation frequencies of the gain block and FIR filter are 16MHz.

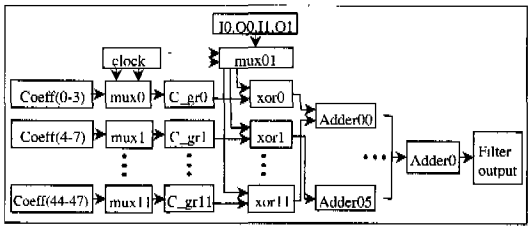

Fig 5 Block diagram of the FIR filter

As mentioned before, the ASIC processes four channels: two I- channels and two Q- channels. The data combiner combines I_0 channel with I_1 channel and Q_0 channel with Q_1 channel. The combined I- and Q- channel output of the ASIC become 10 bits and are sent to D/A chip[4][5].

Ⅳ. Timing of the major signal

System reference clocks of the modulator and the demodulator in the WLL systems are even second and 20ms clock.

For easy synchronization of the data processing with the mobile demodulator, the PN spreading of forward link data starts at the rising edge of 20 ms clock. The data processings which should be done prior to the PN spreading, such as channel coding, block interleaving, scrambling and Walsh modulation, are controlled by the "Back to the future" counter which has the early time calculated from the 20 ms pulse. The DSP can also set an arbitrary offset in timing to determine the relative offset of the forward and reverse links, which is used in the integrated test of the function of the WLL system.

Figure 6 shows the timing simulation of the data receiving block and spreading block of traffic channel. It shows the timing relationships among the 20ms clock and encoder clock and spreading clock. Figure 7 shows the simulated eye diagram of the designed ASIC with random data input, and figure 8 shows the measured eye diagram of the fabricated ASIC chip for modulated signals.

Ⅴ. Implementation

In hardware implementation of the Modulator Channel Card, multiple FPGA's, two modulator ASIC chips and two DSP chips are mainly used. The modulator ASIC was designed and simulated from functional description to layout. Figure 9 shows the overall flow diagram of the modulator ASIC chip design.

The key features of implemented ASIC are as follows.

- Data Rate : 8 - 144Kbps
- PN Chip Rate : 4.096Mcps or 8.192Mcps
- System clock : 32MHz
- Modulation : QPSK/QPSK
- Package : 144 Pin QFP type
- Gate Density : 40,000
- I/O Interface : CMOS level
- Power : +5 Volts
- Technology : 0.6mm CMOS gate array

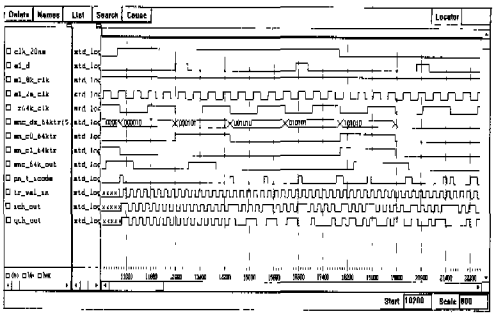

Fig. 6 Timing simulation of channel coding & spreading module of Traffic channel

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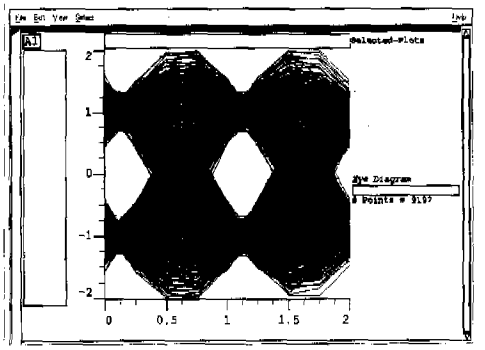

Fig. 7 The simulated eye diagram of the modulator ASIC

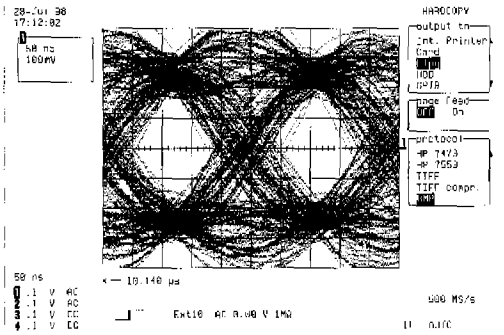

Fig. 8. The measured eye diagram of the modulator ASIC

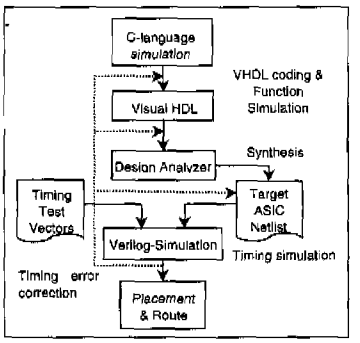

Fig. 9 Design flow of the modulator ASIC

Plot of the designed modulator ASIC chip is shown in figure 10. The function of implemented modulator ASIC is tested and verified with simulation results and functional requirements.

The FPGA block controls the overall board, including ST-bus interface and interrupt control, and is implemented by ALTERA's MAX9560 chips. The 32-bit fixed point Digital Signal Processor is used for high speed processing, which is operated at 50 MHz system clock. One serial communication controller chip is used for RS232 serial communication with external monitor block.

Figure 11 shows the fabricated VLSI ASIC chip and figure 12, the Modulator Channel Card implemented on 6-layer PCB.

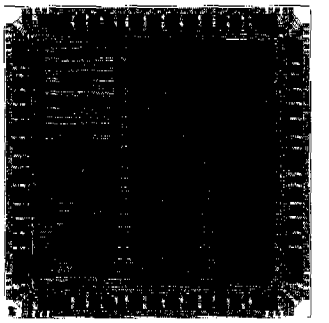

Fig. 10 Plot of the modulator ASIC

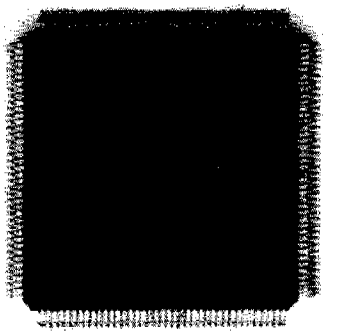

Fig. 11 Implemented VLSI chip

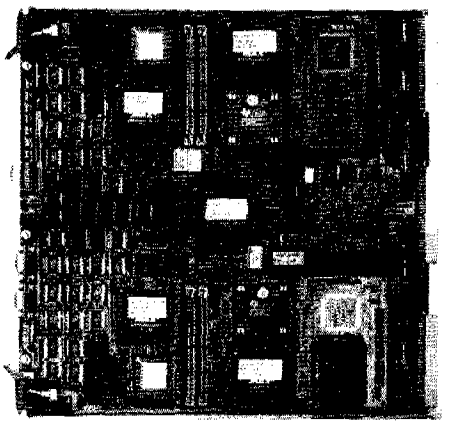

Fig. 12 Implemented Modulator channel card

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Ⅵ. Conclusion

In this paper, we present the functional description, design philosophy and algorithms, implementation issues of the Modulator Channel Card and VLSI chip for the wideband CDMA WLL System. The Modulator Channel Card can operate as any forward link physical channel with a single hardware. And it is also implemented to process four forward link physical channels at a time. The data rates implemented in the Modulator Channel Card are from 32 to 144kbps for traffic channel and 8kbps for control and signaling channel. The ASIC carries out four I- or Q- phase channel signal processing at a time.

The implemented Modulator Channel Card meets functional and performance requirements in itself, and also operates well when it is integrated to the WLL system.

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