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스트레스에 의한 누설전류가 DRAM의 refresh time에 미치는 영향에 관한 연구

정회원 홍 성 희*, 이 재 기**, 김 창 복***

The Impact of Stress Induced Leakage Current on the Refresh Time in DRAM

Sung-Hee Hong*, Jae-Ki Lee**, Chang-Bok Kim*** *Regular Members*

요 약

본 논문은 스트레스에 의한 누설전류(SILC : Stress Induced Leakage Current)의 온도에 대한 종속성과 실제로 동작할 수 있는 조건하에서 스트레스에 의한 누설전류가 Giga-bit 레벨 DRAM의 refresh time에 미치는 영향에 대하여 연구하였다. 스트레스에 의한 누설전류는 monitoring 온도와 스트레스 온도가 증가함에 따라 같이 증가하는 것을 알 수 있었다. 또한 Giga-bit 레벨 DRAM refresh 회로의 SPICE simulation 결과로부터 스트레스 시간에 따른 SILC의 증가가 373K 이하에서의 refresh failure와 고온에서 pn 접합 누설전류에 중요한 영향을 끼침을 알 수 있었다.

ABSTRACT

This paper describes the temperature dependence of stress induced leakage current and its impact on the refresh time in Giga bit level DRAM with practical considerations. SILC has been found to increase as the monitoring and stress temperature increases. From the simulation results of refresh circuit for Giga bit level DRAM, it has been found that the increase of SILC with stress time can be a dominant factor in refresh failure below 373K and pn junction leakage at high elevated temperature.

I. Introdution

SILC is an important concern in scaling gate oxide thickness because it can decrease the DRAM refresh times (T_{ref}), degrade the flash memory data retention, and increase MOSFET off-state power consumption. Although many studies about the conduction mechanism for SILC [1-3] and about the impact of pn junction leakage current (I_j) on T_{ref} [4-5] have so far been performed, the impact of SILC on T_{ref} has not been examined practically.

The purpose of this work is to examine the temperature dependence of SILC and to show practically that T_{ref} for G-bit level DRAM should be determined by not only I_j but also SILC.

II. Device and Techniques

Both MOS capacitors and pn junction diodes with the same area A = 16x10-4cm^2 have been used in this experiment. The gate oxide thickness for MOS capacitors is 5.0nm. MOS capacitors were stressed under constant current stress (J_c = 10 mA/cm^2) at elevated temperature (300K ~

* 여주대학 컴퓨터 정보관리과(shhong@mail.yeojoo.ac.kr) ** 가천길대학 전자통신과(jklee@gcgc.ac.kr)
*** 가천길대학 사무자동화과(cbkim@gcgc.ac.kr)
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423K) and were monitored at different temperature as shown table 1. SILC and I_j have been monitored at V_g = 3.5V and V_j = 2.8V, respectively, which are practical conditions for the half -V_{cc} precharge scheme in Giga-bit DRAM.

Ⅲ. Temperature Dependence of SILC

Fig. 1 shows the temperature dependent SILC behavior of sample S_3. It is found that the SILC at 423K is increased by almost one decade of time as compared to the SILC at 300K. Therefore, the increase of the SILC at elevated temperature will cause a DRAM refresh failure.

Fig. 2 summarized the difference of the stress induced gate leakage current (ΔJ_g) between samples as shown in table 1. ΔJ_{g21}(= J_{gs2} - J_{gs1}) exhibits the effect of monitoring temperature on SILC conduction mechanism. The positive increase of ΔJ_{g21} indicates that the emission of trapped charge is largely enhanced at elevated temperature. ΔJ_{g41} (J_{gs4} - J_{gs1}) exhibits the effect of stress temperature on trap generation.

Table 1. summary of sample capacitors with different stress and monitoring conditions

samples	stress conditions CCS at J = 10mA/cm²	monitoring conditions (Vg = 3.5V)
S_1	Room Temp.	Room Temp.
S_2	Room Temp.	High Temp.
S_3	High Temp.	High Temp.
S_4	High Temp.	Room Temp.

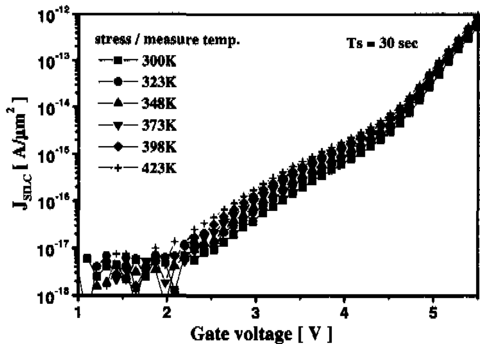

Fig. 1 Temperature dependence of SILC behavior of sample S_3

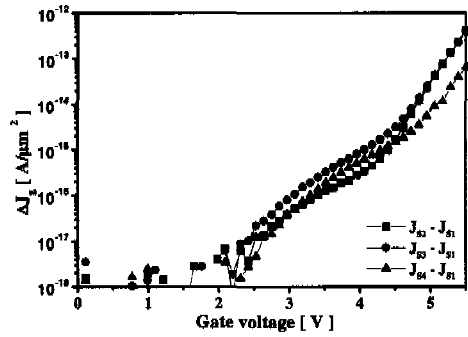

Fig. 2 Difference of SILC between samples

The positive increase of ΔJ_{g41} indicates that the neutral bulk oxide traps and the interface states are largely generated at elevated temperature as ref.[2]. ΔJ_{g31} (= J_{gs3} - J_{gs1}) exhibits the both effects of stress and monitoring temperature and steady state SILC conduction mechanism. The positive increase of ΔJ_{g31} indicates that the increase of SILC following a long time stress at elevated temperature can be the cause of a DRAM refresh failure.

Fig. 3 shows the comparision of leakage current between SILC and I_j with stress time and temperature. At 300K, I_j is larger than SILC. However, SILC becomes larger as the stress time increases. Therefore, SILC can reduce T_{ref} seriously. At above 373K, it is found that I_j is the dominant leakage current in MOSFET devices. Although the leakage current after soft breakdown remains small compared to the high direct tunneling current, there will be totally refresh failure in DRAM, especially after soft breakdown.

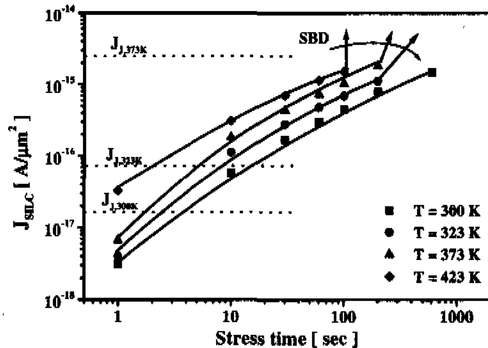

Fig. 3 SILC versus stress time with temperature

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Fig. 4 shows the temperature dependence of SILC and I_j. The activation energy for the SILC is smaller than that for I_j. From this figure, we can also confirm that the increase of SILC with stress time can lead to refresh failure more dominantly than I_j at room temperature.

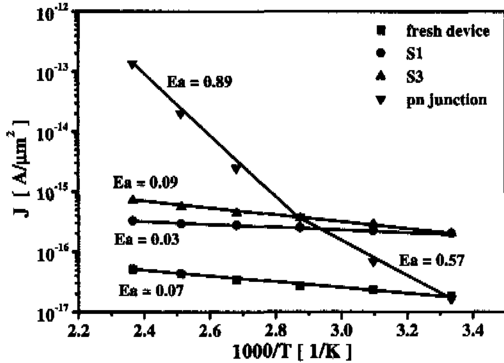

Fig. 4 Temperature dependence of SILC and junction leakage

Ⅳ. The Impact of SILC on T_{ref}

In order to examine the impact of SILC on T_{ref}, the modified refresh circuit as shown in Fig. 5 has been simulated using the SPICE program. The device size of cell transistor has been assumed for Giga-bit level DRAM (W/L = 0.2/0.18㎛) and device parameters for the SPICE simulation have been extracted by BSIM3.

In Fig. 5, the supply voltage V_{cc} and the storage capacitor C_S are 2.8V and 10fF respectively. The leakage current due to SILC has been implemented in parallel with I_j, and the subthreshold leakage current has been neglected here. We also considered the area dependence of I_j because we used large area pn devices for I_j measurement.

Fig. 6 shows the change in C_S voltage versus time before and after constant current stress J_c = 10㎃/㎠ for 600sec at 300K. The T_{ref} has been determined as the time that C_S voltage decreases to $2V_{cc}/3$. From Fig. 6, it is found that T_{ref} decreases from 1.3sec to 22.7msec after stress.

Fig. 7 shows the T_{ref} versus stress time at different stress temperature. We can clearly observe the impact of SILC on the refresh time in DRAM especially at room temperature.

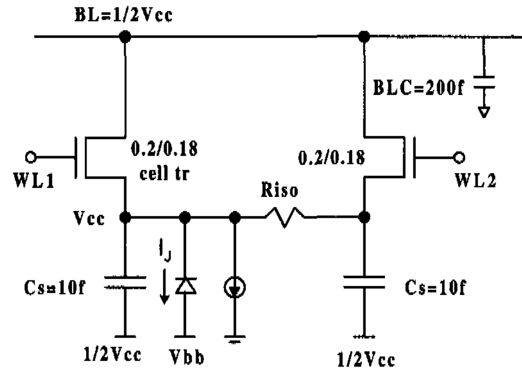

Fig. 5 Schematic diagram of refresh circuit

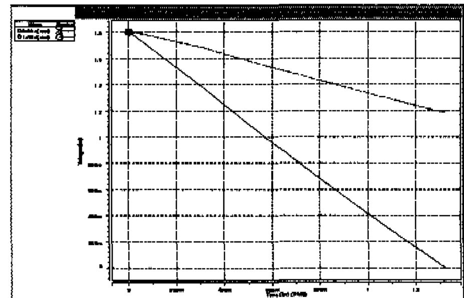

Fig. 6 Change is CS voltage versus time before and after stress

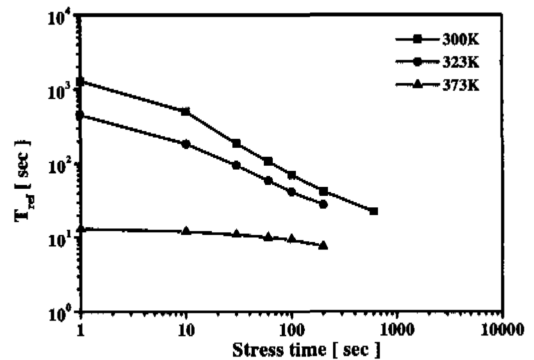

Fig. 7 Tref versus stress time with temperature

V. Conclusion

The effect of stress and monitoring temperature on SILC have been examined. It is found that SILC increases with the monitoring and stress temperature. From the SPICE simulation of

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refresh circuit for Giga-bit DRAM, the increase of SILC is found to give a serious impact on the refresh failure.

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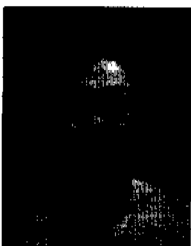
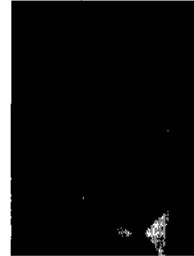
홍 성 희(Sung-Hee Hong) 정회원



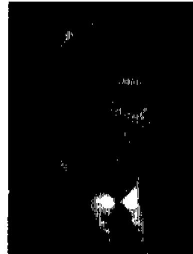
1988년 2월 : 인천대학교 전자공학과 졸업(공학사)
1990년 2월 : 인천대학교 대학원 전자공학과 졸업 (공학석사)
1998년 3월～현재 : 인천대학교 대학원 전자공학과 재학 중(박사과정)
1994년 8월～현재 : 여주대학 컴퓨터 정보관리과 부교수
<주관심 분야> 데이터 통신 및 반도체

이 재 기(Jae-Ki Lee) 정회원



1987년 2월 : 서울산업대학교 전자공학과졸업 (공학사)
1990년 2월 : 인천대학교대학원 (공학석사)
1998년 9월～현재 : 인천대학교 대학원 전자공학과 재학 중(박사과정)
1992년 2월～현재 : 가천길대학 전자통신과 부교수
<주관심 분야> 시스템 설계 및 반도체

김 창 복(Chang-Bok Kim) 정회원



1986년 2월 : 단국대학교 전자공학과 졸업(공학사)
1989년 2월 : 단국대학교 대학원 전자공학과 졸업 (공학석사)
1991년 3월～현재 : 단국대학교 대학원 전자공학과 재학 중(박사과정)
1994년 2월～현재 : 가천길대학 사무자동화과 조교수
<주관심 분야> 웹 프로그래밍 및 neuron-MOS

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