A Monolithic 5 GHz Image Reject Mixer for Wireless LAN applications

Ho-Young Kim*, Jae-Hyun Cho*, Jung-Ho Park* ***Regular Members***

ABSTRACT

A monolithic 5 GHz image reject mixer using a 0.5-m GaAs MESFET technology is designed and simulated. The Mixer exhibits a 13.56 dB down-conversion gain, a SSB (Single SideBand) noise figure of 11.91 dB, an input IP3 (third order intercept point) of -3.73 dBm and a P1dB (1-dB compression point) of -11.0 dBm. The critical issue in the image reject mixer is the phase accuracy and magnitude balance of the 90 phase shifting network. The proposed image reject mixer realizes a 90 phase shifter on chip. This phase shifting network does not need any phase adjusting to achieve the phase error specification of 3 over a frequency range from 800 MHz to 1GHz. The simulated overall image rejection ratio is better than 50 dB.

I. Introduction

The growing popularity of notebook computers demands high data-rate wireless local area network (LAN) systems. Many existing wireless LAN systems operate in the 2.4 GHz ISM band. As various wireless standards continue to populate the 2.4 GHz range, the next step is to extend the communications to the unlicensed 5-GHz band. For example, the Federal Communications Commission (FCC) has released 300MHz of spectrum for the unlicensed national information infrastructure (U-NII)[1]. Currently being drafted is the IEEE 802.11a standard[2] that would make use of these newly allotted frequency bands between 5.15-5.25 GHz, 5.25-5.35 GHz and 5.725-5.825 GHz. Using these newly released frequency bands, wireless LAN systems can provide data rates of several tens of megabits per second. The allocated frequencies overlap the European standard for the high performance radio LAN (HIPERLAN) frequency band.

The superheterodyne architecture is the most widely used architecture for wireless receivers. Monolithic image cancellation has always been a challenge due to the design problems of on-chip filters. The use of image-reject architectures alleviates this problem to some extent. Typically this architecture can achieve 30-40 dB of image cancellation[3],[4]. The image-reject receiver is originally proposed by Hartely[5]. This architecture has two big advantages. First, it eliminates the need for high-Q high-frequency image rejection filters, which must be implemented with external passive components in the superheterodyne architecture. Therefore, the power consumption can be greatly reduced because there is no need to drive the low input impedance off-chip passive filters anymore. Second, intermediate frequency (IF) can be very low because the performance of image rejection does not depend on IF. Therefore, selectivity is sufficient for integrated filters with a Q factor of only 10 to 20, typically. The image reject receiver has found application in radio receivers[6], mobile phone transceivers[7] and video systems[8]. However, it has not become very popular. The critical problem of image reject receiver is the phase error and magnitude

* 고려대학교 전자공학과 광전자 연구실(iamtorn@hanmail.net)
논문번호 : K01210-1009, 접수일자 : 2001년 10월 9일
※ This work was supported by the Korea Research Foundation. ※본 연구는 IDEC MPW의 지원으로 칩이 제작되었습니다.
※ 본 연구에서 제작된 칩은 SSI(Sewon-Semiconductor Incorporation)의 지원으로 packaging 되었습니다.

imbalance generated by phase shifting network, which limits image rejection ratio to only 35dB. In literature, two types of phase shifting networks are described. The first is a frequency doubling with a division by 2 and the second is the combination of the RC integrator and CR differentiator[9]. The first approach is rather power consuming for use in portable systems. The second approach requires trimming to adjust the two RC time constants within specifications. These are the main reasons why, until now, single-chip receivers have integrated all functions except 90 phase shifter. A new approach is demonstrated which shows the possibilities of full integration of image reject mixer without trimming. It is shown that an image rejection of 52.5 dB can be achieved in the frequency range from 800 MHz to 1 GHz.

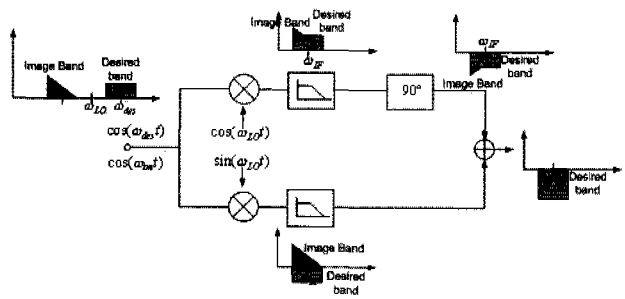


Fig. 1 Principle of image reject receiver

Ⅱ. The Basic Principles and Practical Issues

2.1 The Image Reject Mixer Principles

There are a few descriptions of image reject receiver topology. However, all are similar to the one shown in Fig. 1. It consists of two matched mixers, a 90 phase shifter network, a quadrature local oscillator (LO), and a summing circuit.

Fig.1 also illustrates the operation principle of the image reject receiver. Here, the quadrature signal is defined to lead in-phase signal by 90° , and phase shifting is defined to shift phase in advance. The image signal lies at $\omega_{RF}-2\omega_{IF}$ for system having ω_{LO} lower than ω_{RF}. In this receiver, the desired and image signal are mixed down together in both signal paths. However, the desired signal at the end, the upper and the lower paths are in-phase, while image signals are 180° out of phase. When the upper path and the lower path are recombined, the image signal will be cancelled out and the desired signal left.

To understand principle, suppose the input signal is $x(t)=A_{RF}\cos(\omega_{RF}t)+A_{im}\cos(\omega_{im}t)$, where the first term represents the desired channel and the second term the image. Without loss of generality, we assume low-side injection:

$$\omega_{RF}-\omega_{LO}=\omega_{LO}-\omega_{im}.$$

For a perfectly matched circuit, the signal at node A is

$$x_A(t)=A_{RF}\cos(\omega_{RF}t)\cos(\omega_{LO}t)+A_{im}\cos(\omega_{im}t)\cos(\omega_{LO}t)$$
$$=\frac{A_{RF}}{2}\cos(\omega_{IF}t)+\frac{A_{im}}{2}\cos(\omega_{IF}t)$$

(low-passed)

at node B is

$$x_B(t)=\frac{A_{RF}}{2}\cos(\omega_{IF}t+90^\circ)+\frac{A_{im}}{2}\cos(\omega_{IF}t+90^\circ)$$
$$=-\frac{A_{RF}}{2}\sin(\omega_{IF}t)-\frac{A_{im}}{2}\sin(\omega_{IF}t),$$

at node C is

$$x_C(t)=A_{RF}\cos(\omega_{RF}t)\sin(\omega_{LO}t)+A_{im}\cos(\omega_{im}t)\sin(\omega_{LO}t)$$
$$=-\frac{A_{RF}}{2}\sin(\omega_{IF}t)+\frac{A_{im}}{2}\sin(\omega_{IF}t)$$

(low-passed)

Therefore, the output signal from the image reject mixer is $-A_{RF}\sin(\omega_{IF}t)$, and the image signal is cancelled out.

In practice, the 90° phase shift is replaced with a +45° shift in one path and a -45° shift in the other. (Fig. 2)

The principal drawback of Hartely's architecture (Fig. 2) is its insensitivity to mismatches. If the

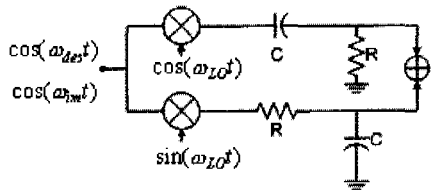


Fig. 2 Image reject receiver with split phase shifter stages

LO phases are not in exact quadrature or the gains and phase shifts of the upper or lower paths in Fig.2 are not identical, then the cancellation illustrated above is incomplete and the image corrupts the downconverted signal[10].

Suppose that the total gain mismatch (or ratio of gains) and phase error in the two paths of the image reject receiver are ε and θ degree, respectively. The IRR (Image Rejection Ratio) is given by:

$$IRR = \frac{1 + 2\varepsilon\cos\theta + \varepsilon^2}{1 - 2\varepsilon\cos\theta + \varepsilon^2}$$

Factors, which limit the IRR in the real IC systems, are (1) gain difference between two mixers, (2) magnitude imbalance and phase error between the quadrature outputs of LO, and (3) magnitude imbalance and phase error of the phase shifting network in the signal path.

A more critical problem is the magnitude imbalance and phase error of the phase shifting network in the signal path. In the following subsection, existing methods of phase shifting network design will be briefly reviewed.

2.2 The Phase-Shifting Network

There are many types of phase shifting networks in the literature: delay lines[11], distributed couplers, lumped LC couplers[12], digital frequency dividers[13] and RC/CR allpass network [14]. However, only RC/CR allpass networks are commonly used in image reject receivers, because the other methods are not suitable for monolithic integrated circuits.

In a RC/CR network, the output of a RC low pass section has always a 90° phase leg from a CR high pass section. The phase error comes from the RC relative value variance, which can be well controlled. The major drawback is that its magnitude response is only well matched at $f=1/(2\pi RC)$, and this frequency depends on the absolute RC value, which may have up to 50% variance for a typical IC technology. Thus, the achieved IRR is limited to about 20 dB only. A solution to the problem of center frequency variance is to use tunable RC/CR circuit where the value of R or C is controlled by an external voltage[15].

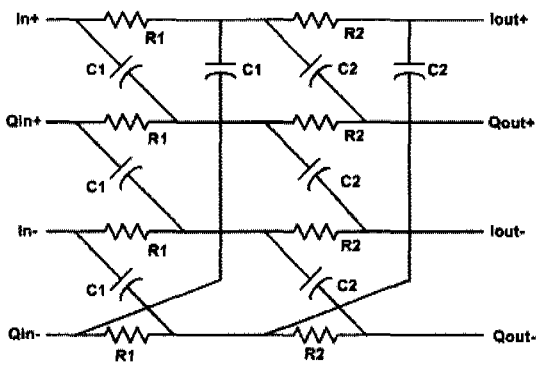


Fig. 3 Two stage polyphase network

Recently, the sequence asymmetric cascaded RC polyphase network was proposed, which yields a phase error of 0.5° and a magnitude imbalance of 0.5dB[16] (corresponding to 31dB IRR) in a wide frequency range. (Fig. 3) This method can select the band range by cascading multi-stage since the rule of thumb for polyphase networks say that each stage provides reasonably constant gain over roughly a 10% bandwidth[17]. For example, to design for an 1 GHz center frequency, one might choose RC for the first stage to correspond to 900 MHz, while RC for the second stage might be selected to correspond to about 1.1 GHz. A significant disadvantage of this network, however, is its attenuation and noise.

In this circuit, a signal and its inverse are applied to one pair of input pins, with the other two pins are grounded. Due to its asymmetric structure, the magnitude error in RC section will be compensated in the next CR section. Therefore, with quite mild tolerances on its

components, it is possible to have an order-of -magnitude improvement in magnitude response over the RC/CR network. The RC polyphase network is suitable for frequencies higher than 10MHz for reasonable chip area consumption.

Ⅲ. Proposed Architecture and Simulated Results

3.1 Architecture

If the basic scheme of an image reject mixer is analyzed (see Fig. 1), it can be seen that it consists of a first multiplier and a second multiplier with a phase shifter in the back of it. Fig.4 shows a designed mixer and an output buffer amplifier.

By analyzing the structure more in detail it can be noticed that the mixer output voltage Vin is converted into a current by a differential pair with the emitter degeneration resistor R. In other words, the voltage is in first order converted into a current given by Ohms law $\Delta I = V_{in}/R$. If the resistor R is now replaced by a capacitor, this relationship becomes $\Delta I = j\omega C \cdot V_{in}$, and hence, in the ideal case, the current is now 90° phase shifted. As a result, to realize the second mixer including phase shifter, only one resistor in Fig. 4(a) is replaced by a capacitor as is shown Fig. 4(b). So the phase shifting is realized.

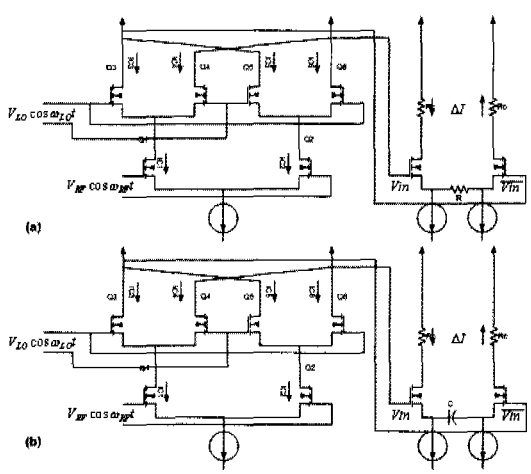


Fig. 4 (a) Circuit diagram of the mixer and buffer amplifier (b) the mixer with the 90° phase shifter

Both circuits (Fig. 4(a), (a)) can be analyzed by their small signal equivalent. (Fig. 5)

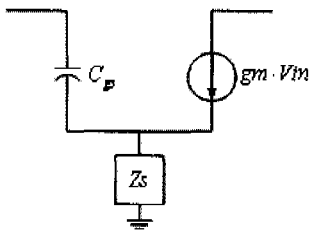


Fig. 5 Input impedance model: Zs

$$Z_{in} = \frac{1}{j\omega C_{gs}} + Z_s + \frac{\omega_T}{j\omega} Z_s$$

The equation above for input impedance was derived from a simple small-signal analysis neglecting Cgs and assuming that the node between the source resistors is at virtual ground. (Note: $\omega_T = gm/C_{gs}$)

As shown in Table 1, the outputs of the circuits have ideally a phase difference of 90° . In order to reduce the gain difference between two circuits in the frequency range of interest, R and C are designed to have an equal gain in the middle of the frequency range. This can be expressed by $R = \frac{1}{2\pi fC}$.

Table 1. Input impedance of the mixer

Zs	Re[Zin]+Im[Zin]
R	$R + (\frac{\omega_T R}{j\omega} + \frac{1}{j\omega C_{gs}})$
L	$\omega_T L + (\frac{1}{j\omega C_{gs}} + j\omega L)$
C	$-\frac{\omega_T}{\omega^2 C} + (\frac{1}{j\omega C_{gs}} + \frac{1}{j\omega C})$

In real circuit, however, it is not enough to make 90° phase difference by this method. In order to increase the phase difference to 90° , the capacitance must be decreased. Then, the conversion gain of the mixer will be abruptly reduced. And the resistance will be increased, which may increase the chip size. Therefore, in newly developed mixer, we replace R with L.

(Fig. 6)

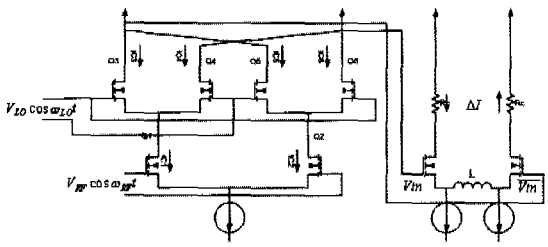


Fig. 6 Circuit diagram of the designed image reject mixer

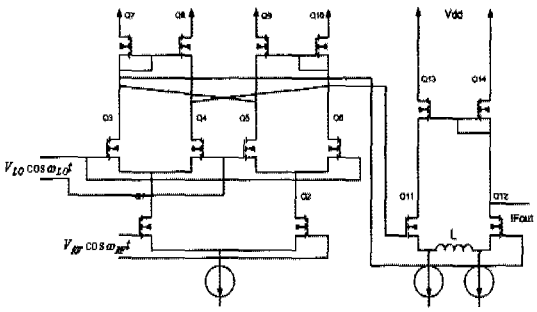


Fig. 7 Circuit diagram of the down-conversion mixer cell

Inductor can provide sufficient phase difference. Besides, conversion gain reduction of the mixer will be effectively decreased. And It can be easily shown that a differential pair output buffer stage with reactive (inductive or capacitive) degeneration has lower NF (noise figure) than that with resistive degeneration, since the degeneration reactance (apart from its loss resistance) does not introduce an additional noise source.

3.2 Simulation Result

The circuit diagram of the down-conversion image reject mixer cell is shown in Fig. 7. A traditional four-quadrant Gilbert mixer is used[18]. It consists of transconductance stage (Q1-Q2), differential switching pairs (Q3-Q6), load (Q7-Q10, Q13-1Q4) and output buffer stage (Q11-Q12).

The transconductance stage generates currents in proportional to RF signal. The differential switching pairs perform the chopping operation of the current output of the transconductance stage and thus down-convert the RF signal into the IF band. In order to drive differential pairs sufficiently to be turned on/off, the LO signal strength should be large enough. The cross-coupled load (Q8-Q9) is placed in parallel with the diode-connected load (Q7, Q10). This configuration yields very low resistance level for common mode signal whereas the resistance for differential signal is high. So, the common-mode feedback circuit is not required as in conventional circuits using active load. In such circuits, the MESFET load transistor is usually connected as a constant-current source and thus presents the amplifier transistor with a very-high-resistance load (the output resistance of the current source). Thus amplifiers that utilize active loads can achieve higher voltage gains than those with passive (resistive) loads.

The design of this image reject mixer uses nonlinear microwave simulator HP ADS developed at Agilent EEsof EDA. The simulation result of the scheme is summarized in Table 2.

Table 2 Simulated results of the image reject mixer

Parameter	Unit	Specifications
Conversion Gain	dB	13.56
Noise Figure	dB	11.91
1dB compression point(P1dB)	dBm	-11.0
Input IP3	dBm	-3.75
Image Rejection Ratio	dB	52.5

Fig. 8 shows IF output spectrum. The 5.25 GHz -30 dBm RF signal is downconverted to the 900 MHz -16.44 dBm IF signal. A down conversion gain of 13.56 dB was achieved for a 5.25 GHz RF and 900MHz IF.

In a wireless LAN system, the receiver must be sensitive enough to detect signals as small as -148 dBm/Hz. (i.e., -74 dBm for a 24 MHz bandwidth signal[19]) To have a pre-detection signal-to-noise-ratio (SNR) of at least 12 dB, the overall noise figure of the receiver must be better than

$NF = -148dBm/Hz - 12dB - (-174dBm/Hz) = 14dB$,

where -174 dBm/Hz is the available noise power

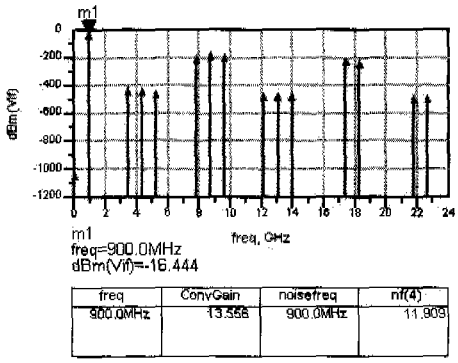


Fig. 8 Mixer output spectrum, conversion gain, and noise figure

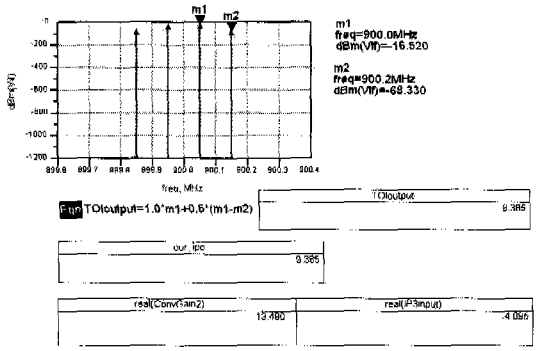


Fig. 10 Third-order intercept point
(RF1=5.25GHz+50kHz, RF2=5.25GHz-50kHz)

of the source. The noise figure of this mixer is 11.91 dB. This number is lower than 14 dB.

For the linearity, an input 1dB compression point of -11.0 dBm (Fig. 9), and an input third order intercept point of -3.75 dBm (Fig. 10) were resulted.

In-band and out-of-band blockers usually limit the performance of the receiver. For a wireless LAN receiver, the in-band blockers (adjacent channels) are the most important blockers that limit the performance of the system. To measure the effect of in-band blockers, a 1-dB in-band blocking simulation is performed. Assuming a channel width of approximately 24 MHz, a single in-band blocker is applied at 24 MHz offset from the carrier. The power of the blocker is increased until a 1-dB reduction in the output signal is observed. According to the simulated results, the 1-dB in-band blocking de-sensitization occurs when the power of the blocker is -15 dBm. This

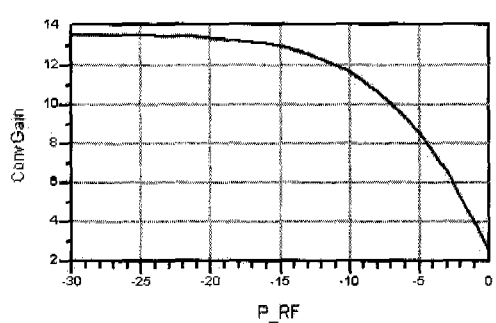


Fig. 9 Down-conversion Gain vs. input power for the receiver

number is higher than the maximum power of the adjacent channel (-20 dBm), so the in-band blocking performance is more than adequate.

The desired band RF signal (5.25-5.35 GHz) and image band signal (3350-3450 MHz) are down-converted to IF band (900MHz). The desired IF band signal (900 MHz) and image IF signal (900.01MHz) are shown in Fig. 11, and image signal is suppressed by 52.5dB.

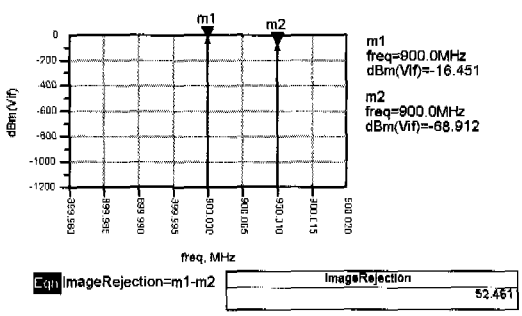


Fig. 11 Simulated image rejection ratio

Ⅳ. Conclusions

A monolithic 5 GHz image reject mixer using a 0.5-m GaAs MESFET technology is designed, simulated and fabricated. The die photos of the image reject mixer is shown in Fig. 12. Adoption of the image-reject architecture eliminates an RF filter and its associated I/O interface in a heterodyne receiver, thereby reducing overall cost.

The critical problem of image reject mixer is the phase error and magnitude imbalance

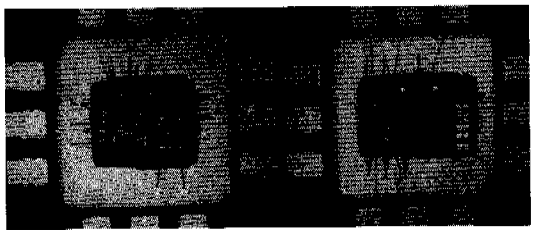


Fig. 12 Image reject mixer micrograph

generated by phase shifting network, which limits image rejection ratio to only 35dB. A new approach is demonstrated which shows the possibilities of full integration of image reject mixer without trimming. It is shown that an image rejection of 52.5 dB can be achieved in the frequency range from 800 MHz to 1 GHz.

References

[1] K. Pahlavan, A. Zahedi and P. Krishnamurthy, "Wide band local access: wireless LAN and wireless ATM", *IEEE Communication Magazine,* pp. 34-30, Nov. 1997

[2] IEEE 802.11a Draft Supplement to IEEE Std 802.11,Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: High Speed Physical Layer in the 5 GHz band, Draft 7.0, July 1999

[3] B. Razavi, "Design Considerations for Direct-Conversion Receivers", *IEEE Trans. on circuits and systems*, vol. 44, pp 428-435, June 1997

[4] M. McDonald, "A 2.5GHz BiCMOS image-reject front-end", *ISSCC Dig. Tech. Papers*, pp. 144-145, Feb. 1993

[5] R. V. L. Hartely, "Modulation System", *U. S. patent,* no. 1, pp 206, Apr. 17 1928

[6] H. Tomiyama T. Okanobu and H. Arimoto, "Advanced low voltage single chip radio IC", *IEEE Trans. Consumer Electronics*, vol. 38, no.3, pp. 465-475, August 1992

[7] Philips Semiconductor, *Philips RF/ wireless communications data book.*, 1996

[8] J. Granlund John W. Archer and R.E.Mansy, "A broadband UHF mixer existing high image rejection over a multi decade baseband frequency range", *IEEE J. Solid-State Circuits*, vol. SC-16, no.4, pp 385-392, August 1981

[9] P. H. Saul, "Monolithic silicon RF circuitry-Current achievement and future potential", *Proc. IEEE ESSCIRC*, pp 25-28, Sept. 1990

[10] Behzad Razavi, *RF Microelectronics* , Prentice Hall, 1998

[11] Bois, J.R.; Bobot, H.; Ouvrard, P.L.; Lazar, S., "A Wide Band Gaas Mmic Delay Line Phase Shifter with On-Chip Drivers", *Microwave Conference 1992, AMPC '92, Asia-Pacific*, Vol.1, pp. 283 -286, 1992

[12] Al-Anwar, H.I.; Motawe, I.M.; El Hennawy, H.; Mahrous, S., "A new method for the design and synthesis of broadband constant phase shift microwave hybrid couplers", *Radio Science Conference, 1998. NRSC '98. Proceedings of the Fifteenth National*, pp. B17/1-B17/15, 1998

[13] Lovalace, D.; Durec, J., "A self calibrating quadrature generator with wide frequency range", *Radio Frequency Integrated Circuits (RFIC) Symposium, 1997., IEEE*, pp. 147 -151, 1997

[14] H. M. Rein et al., "A 3Gb/s bipolar phase shifter and AGC amplifier.", *ISSCC Dig. Tech. Papers (Sanfrancisco, CA)*, pp 145-145, Feb. 1989

[15] M. Ishikawa T.Tsukahara and M. Muraguchi, "A 2V 2GHz Si-bipolar direct-conversion quadrature modulator", *IEEE J. Solid-State Circuits*, vol. 31, no. 2, pp 262-267, Feb. 1996

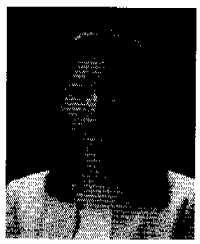
[16] J. Crols and M.Steyaert, "A fully integrated 900 MHz CMOS double quadrature downconverter", *ISSCC Dig. Tech. papers*, pp 136-137, 1995

[17] Thomas H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* , Cambridge University Press, 1998

[18] B. Gilbert, "A precise four quadrant multiplier with subnanosecond response", *IEEE. J. Solid-State Circuits*, vol. SC-3, pp365-373, Dec. 1968

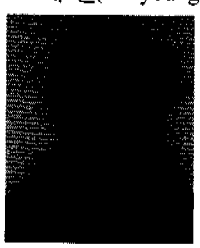
[19] S. Jones, "RF system requirements for HIPERLAN", *Microwave and RF Conference Proceedings*, pp. 1-6, 1995

김 호 영(Ho-young Kim) 정회원



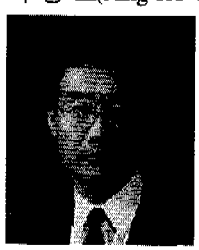
2000년 2월 : 고려대학교 전자공학과 졸업
2000년 3월~현재 : 고려대학교 전자공학과 석사과정
<주관심 분야> 통신공학, MMIC 설계, RF IC

조 재 현(Ho-young Kim) 정회원



2000년 8월 : 고려대학교 전자공학과 졸업
2000년 9월~현재 : 고려대학교 전자공학과 석사과정
<주관심 분야> 통신공학, MMIC 설계, RF IC

박 정 호(Jung-Ho Park) 정회원



1981년 2월 : 고려대학교 전자공학과 졸업
1987년 12월 : University of Delaware 박사
1987년 12월~1990년 2월 : 금성사 중앙연구소 연구실장
1990년 3월~현재 : 고려대학교 전기전자전파공학부 교수
<주관심 분야> 광소자, 반도체공학, MMIC