VBIC Model Application and Parameter Extraction and Optimization for SiGe HBT

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ABSTRACT

In 1995, a group of representatives from the integrated circuits and computer-aided design industries presented a industry standard bipolar model called the VBIC model. The VBIC model includes the improved Early effect, quasi-saturation, substrate parasitic, avalanche multiplication, and self-heating which are not available in the conventional SGP model. This paper applies VBIC model for SiGe HBT device and develops an accurate and efficient methodology to extract all the DC and AC parameters of the VBIC model for SiGe HBT device at room temperature. Simulated results by the extracted VBIC model parameter are compared with the measurement data and show very good agreement in both DC and s-parameters prediction.

Key Words : VBIC, Gummel-Poon, SiGe HBT, Parameter extraction, Parameter optimization.

Ⅰ. Introduction

The SiGe hetero-junction bipolar transistor (HBT) has been considered to be more suitable for RF integrated circuits than the Si bipolar junction transistor (BJT) because its electrical properties, such as current gain, power consumption, and small-signal unity-gain frequency, are superior to those of the Si BJT [1].

Users of the SPICE Gummel-Poon (SGP) model, which has been the industry standard bipolar transistor model for over 20 years, have found it to be inadequate in representing many of the physical effects important in modern advanced and scaled bipolar transistors. In 1995, a group of representatives from the integrated circuits and computer-aided design industries have collaborated and developed a new industry standard bipolar model called the vertical bipolar inter-company (VBIC) model [2,3]. The VBIC model was developed in similar to the SGP model and overcomes its major limitations. The advantages of the VBIC model include correct implementation of the Early effect, improved static temperature modeling, an improved forward-biased junction capacitance option, inclusion of overlap capacitance, Kirk high-current modeling, improved high-level diffusion capacitance modeling, inclusion of substrate transistor with Rc and variable beta, approximation accounting for distributed effects in the input circuit, consistent treatment of excess phase in transient and small signal analyses, models of weak avalanche effect, etc. [4].

Although an improved accuracy of the VBIC model over the SGP model has been demonstrated, procedure and steps for the extraction and optimization of the VBIC model parameters were not nearly discussed. In this

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paper, we applies VBIC model, which was developed for silicon BJT, for compound semiconductor SiGe HBT device and seeks to develop an accurate and efficient methodology to extract all the DC and AC parameters of the VBIC model for SiGe HBT. Simulated results using the extracted parameters of SiGe HBT device will be compared with measurement data. The emitter area of SiGe HBT device used in extraction of model parameters is 0.5x6.0μ m^2, which was fabricated by Electronics and Telecommunications Research Institute (ETRI), Korea. The forward DC current gain, cutoff frequency, and maximum oscillation frequency of fabricated SiGe HBT device are about 160, 40GHz and 30GHz, respectively, and the extracted model parameters will be used in design of 5.8GHz DSRC (Dedicated Short Range Communication) communication for ITS (Intelligent Transportation Systems).

II. Extraction and Optimization of VBIC Model Parameters for SPICE Simulation

The equivalent circuit of VBIC model is shown in fig. 1. Unlike the SGP model, which has three terminals, the VBIC model is a four-terminal model comprising the base (b), emitter (e), collector (c), and substrate (s). The other nodes in VBIC model are the extrinsic base bx, parasitic base bp, intrinsic base bi, intrinsic emitter ei, intrinsic collector ci, and extrinsic collector cx. The VBIC model includes the following features that make it distinct from the SGP model. First, the effect of parasitic substrate PNP transistor was included by a simplified SGP model. Second, the quasi-saturation behavior was modeled with the elements R_{CI}, Q_{bcx}, and modified Q_{bc}. Third, the effect of excess phase was modeled with a second-order sub-network through delay time TD which makes consistent small-signal to transient analysis. Fourth, in addition to the conventional strong avalanche

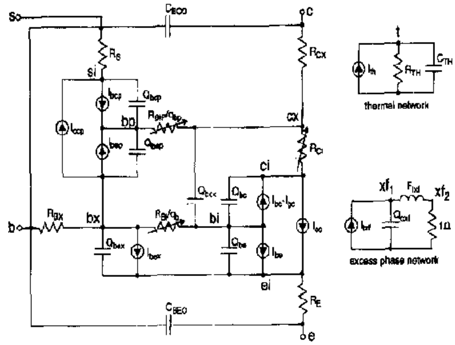

Fig. 1. Equivalent circuit for VBIC bipolar transistor model.

current, a weak avalanche current I_{gc} was added for the base-collector junction. Fifth, to account for the extrinsic capacitances associated with the regions in which the p$^+$ base and n$^+$ emitter are overlapped, two constant capacitances C_{BE0} and C_{BC0} were included in the VBIC model. Finally, a self-heating model was included as a separate option for the VBIC. The model consists of the thermal resistance R_{TH} and capacitance C_{TH}, along with the thermal power source I_{th}, which couples the power generated in the bipolar transistor to the thermal network. The local temperature rise at node t in the thermal network is linked to the electrical model through the temperature mappings of the model parameters [3,4].

To extract and optimize model parameter, the DC measurement was carried out using HP4145/4142 semiconductor parameter analyzer while junction capacitances were measured as function of voltage using HP4280A semiconductor/component test system. Also, AC measurement was performed using HP8510B vector network analyzer. The forward DC current gain, cutoff frequency, and maximum oscillation frequency of the SiGe HBT device with 0.5x6.0μ m^2 emitter area are about 160, 40GHz and 30GHz, respectively, and the extracted model parameter will be used in design of 5.8GHz DSRC communication for ITS. The device was fabricated by 0.8μ m SiGe BiCMOS line of Electronics and Telecommunications Research

Institute (ETRI), Korea.

The VBIC model parameter extraction and optimization method developed in this paper was performed using UTMOST III modeling framework [5]. Fig. 2 shows the overall flowchart of the VBIC model parameter extraction and optimization procedure we have developed for SiGe HBT. The steps for extracting and optimizing VBIC parameters of SiGe HBT device are listed and discussed as follow.

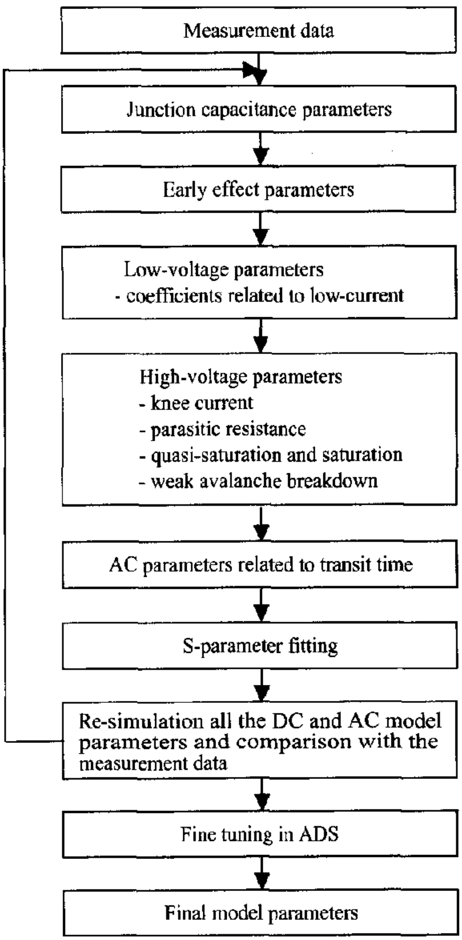

Fig. 2. Flowchart for VBIC model parameter extraction and optimization of SiGe HBT.

2.1 Junction capacitance parameters

In the VBIC model, the parameters associated with junction capacitance are first extracted. The junction capacitance parameters are extracted using capacitance-voltage (C-V) measurement data. The depletion capacitance data should be taken in a forward bias condition up to a point till the diffusion capacitances kicks in. From measured C_{be} versus V_{be} data, in reverse bias and low forward bias regions, CJE, PE, and ME are extracted and optimized. From measured C_{bc} versus V_{bc} data, in reverse bias and low forward bias regions, CJC, CJEP, PC, and MC are extracted and optimized. From measured C_{sc} versus V_{sc} data, in reverse bias and low forward bias regions, CJCP, PS, MS are extracted and optimized.

2.2 DC parameters

The steps for extracting and optimizing VBIC DC model parameters of SiGe HBT are discussed as follow.

As a first step of DC parameter extraction, forward and reverse early voltages (VEF, VER) are extracted and optimized using previous junction capacitance parameters. Physically, the Early voltage accounts for the account of base-width modulation due to change in the collector-base reverse voltage. As the Early voltage approximation to avoid numerical problems in the SGP model was known to have inaccuracies in Early effect modeling, junction depletion charge was introduced in the VBIC model. Forward and reverse early voltages (VEF, VER) for low bias condition are obtained using the following equations [6].

$$\left(q_{j,bc}^{f}-\frac{C_{j,bc}^{f}I_{c}^{f}}{g_{0}^{f}}\right)\cdot\frac{1}{V_{ef}}+q_{j,be}^{f}\cdot\frac{1}{V_{er}}=-1$$

$$q_{j,bc}^{r}\cdot\frac{1}{V_{ef}}+\left(q_{j,be}^{r}-\frac{C_{j,be}^{r}I_{e}^{r}}{g_{0}^{r}}\right)\cdot\frac{1}{V_{er}}=-1 \quad (1)$$

Here, superscripts f and r denote forward and reverse modes, respectively, and g_0 is the output conductance which can be determined from the forward and reverse output characteristics at fixed low-bias V_{be} and V_{bc} since the Early effect model was developed under low injection condition. In equation (1), q_j is the junction charge and c_j is the junction capacitance which is calculated from the junction capacitance-voltage measurement.

As a second step, low voltage parameters of Gummel plot are extracted and optimized. From the forward Gummel plot, IS, NF, IBEI, NEI, IBEN, and NEN parameters are extracted and optimized. Next, from the reverse Gummmel plot, NR, IBCI, NCI, IBCN, NCN, ISP, WSP, NSF, IBEIP, and IBENP are extracted and optimized. Note that the parameters extracted include the parasitic PNP transistor current components [7].

As a third step, high voltage parameters of Gummel plot are extracted and optimized. (1) Knee current parameters (IKF, IKR) are obtained by taking extrapolated intercept point of low-current and high-current curves from the forward and reverse Gummel plots, respectively, and their values are optimized later together with other parameters. (2) The resistor parameters RE and RCX are obtained from the flyback measurement, respectively. The base resistances RBX and RBI are obtained from the forward Gummel plot at high voltages while the parasitic resistances RBP and RS are extracted from the reverse Gummel plot. Then, these extracted resistance parameters are optimized, together with the knee currents extracted previously. (3) The parameters associated with quasi-saturation effect can be extracted from the forward current-voltage characteristics under quasi-saturation and saturation operations. They include the series resistances RCX and RCI, and quasi-saturation parameters VO, GAMM, and HRCF. (4) Next, based on the current-voltage characteristics in avalanche breakdown region, the extraction and optimization of the parameters AVC1 and AVC2 associated with forward weak avalanche breakdown and parameters AVE1 and AVE2 associated with the reverse weak avalanche breakdown are performed.

2.3 AC parameters

To extract AC parameters, the s-parameter measurements (in the range of 500MHz to 10GHz frequency) were carried out using a model HP8510B vector network analyzer at room temperature. The parasitic components associated with the resistance, inductance, and capacitance of the probes, device pads and interconnects are de-embedded. Transit time τ_F is commonly determined from the cutoff frequency f_T measurement. The cutoff frequency f_T is determined by extrapolating h21 parameter transformed from measured s-parameter and parameters related to transit time are extracted from f_T-I_C curve shown in fig. 3.

In this paper, the methods of AC parameter extraction and s-parameter fitting are summarized as follow. Firstly (f_T-I_C curve fitting), since Region I of fig. 3 is dominated by depletion capacitance, initial depletion capacitance parameters optimized in section 2.1 are optimized again, in Region I, to exactly fit f_T-I_C curve and s-parameters. Secondly (parameter optimization associated with transit time), AC parameters associated with transit time are extracted mainly, in Region II of f_T-I_C curve of fig. 3. Finally (s-parameter fitting), as some parameters are voltage-dependent and/or current-dependent (or not linear), s-parameter fitting cannot be done satisfyingly in all bias points. Because of this reason, s-parameter fitting is performed in specific bias point, i.e. optimum bias point considering speed and power indicated fig. 3. In addition to, initial parasitic resistance parameters (RBX, RE, RCX, RBI) optimized in the previously two steps of this section are used simultaneously in s-parameter fitting step

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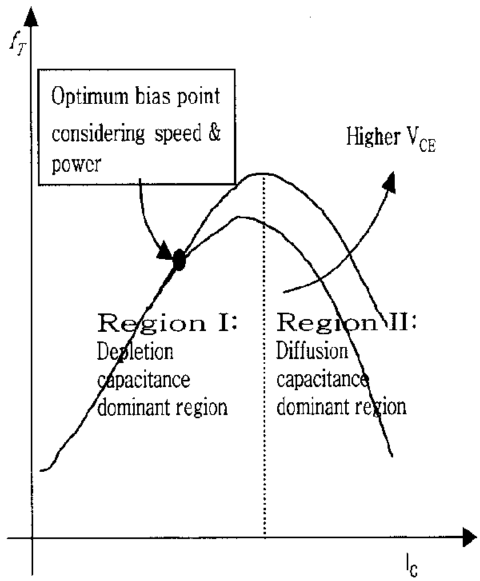

Fig. 3. Variation of cutoff frequency with collector current.

2.4 Overall parameters optimization

At this step, all the extracted DC and AC parameters are optimized simultaneously carefully to get the most accurate DC and AC prediction and finally, all the SiGe HBT VBIC DC/AC parameters extracted previously are tuned again with circuit simulator, ADS (version 2001).

III. Results and Discussion

Fig. 4 compares the DC measurement data and simulation results of the current-voltage characteristics, Gummel plot, current gain under forward operation of SiGe HBT. Fig. 5 and fig. 6 show small-signal s-parameters, S11, S21, S12, S22 traces under V_{CE}=1.0V, I_C=1mA and V_{CE}=2.0V, I_C=1mA for SiGe HBT, respectively.

For DC optimization, average error between measurement and modeled results was below 15 % and for AC s-parameter optimization, average error between measurement and modeled results was below 5 %. As a result

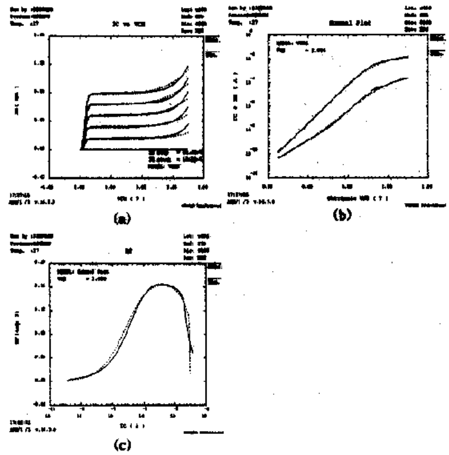

Fig. 4. Comparison of measured and simulated DC results under forward operation of SiGe HBT. (a) Current-voltage characteristics, (b) Gummel plot, (c) current gain. (line: measured, dot: simulated)

of these, the simulation results were in very good agreement with the measurement data and, we can conclude that the extraction and optimization methodology of this paper is very adequate for SiGe HBT modeling using the VBIC model.

IV. Conclusions

The VBIC model includes the improved Early effect, quasi-saturation, substrate parasitic, avalanche multiplication, and self-heating which are not available in the conventional SGP model. In this paper, we have applied the bipolar junction transistor model, VBIC model for SiGe HBT device and presented an accurate and efficient methodology to extract and optimize all the DC and AC parameters of the VBIC model for SiGe HBT at room temperature. Simulated results by extracted VBIC model parameters showed very good agreement with both measured DC and s-parameters data. These results show that the VBIC model can overcome the problem that accuracy in modeling SiGe HBT using the conventional SGP model is decreased. Parameter extraction related to temperature modeling which is one of important characteristics in the VBIC model is yet not performed, but we intend to develop methodology in the near future.

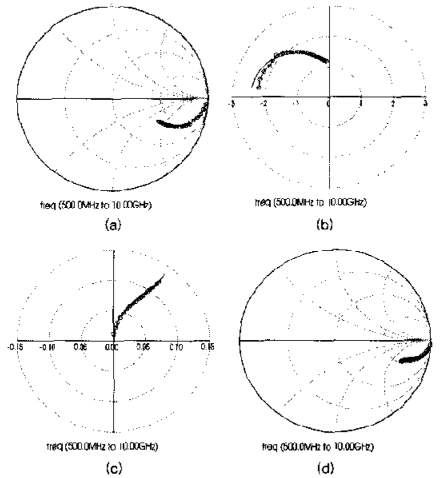

Fig. 5. Comparison of measured and simulated s-parameters under V_{CE}=1V, I_C=1mA for SiGe HBT. (a) S11, (b) S21, (c) S12, (d) S22. (circle: measured, line: simulated)

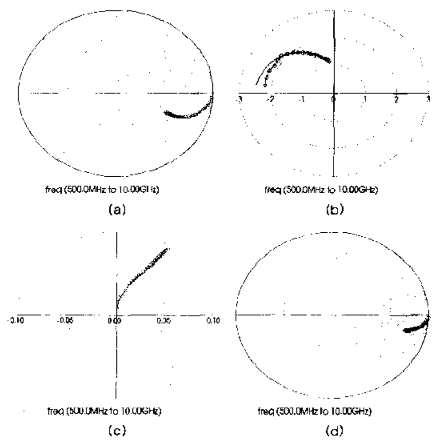

Fig. 6. Comparison of measured and simulated s-parameters under V_{CE}=2V, I_C=1mA for SiGe HBT. (a) S11, (b) S21, (c) S12, (d) S22. (circle: measured, line: simulated)

Acknowledgments

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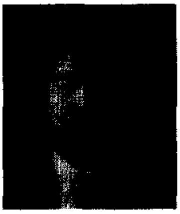

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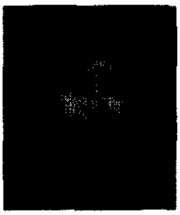

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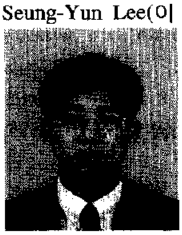

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