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온도가 SOI DTMOS와 PD-SOI MOSFET에 미치는 영향에 관한 연구

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Study on Impact of Temperate on SOI DTMOS and PD-SOI MOSFET

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요 약

본 논문은 다양한 온도에 따라 SOI DTMOS 소자와 PD-SOI MOSFET소자의 특성을 실험적으로 측정하여 분석하였다. DTMOS 소자의 온도에 따른 drive current 및 transconductance 증가에 대한 물리적 메카니즘을 측정된 결과로부터 제안하였다. 또한 온도에 따른 문턱전압, 단채널 현상 및 subthreshold 특성 변화를 측정 결과를 통하여 분석한 결과, 온도가 증가함에 따라 PD-SOI MOSFET 소자에 비하여 DTMOS 소자의 drive current 및 transconductance가 더 크며, 단채널 현상은 줄어들고, subthreshold 특성이 더 좋음을 알 수 있었다.

Key Words : SOI DTMOS, PD-SOI MOSFET, Drive Current, Transconductance, Subthreshold

ABSTRACT

This paper reports that the characteristics of SOI Dynamic-Threshold MOS(DTMOS) transistors are experimentally investigated at various temperatures and compared with those of partially depleted(PD) SOI MOSFET. A possible physical mechanism explaining the enhanced drive current and transconductance of DTMOS devices is suggested from the measured results. The temperature dependence of threshold voltage, short channel effects, and subthreshold characteristics are investigated experimentally. From the comparison with partially depleted SOI MOSFET, it is observed that DTMOS devices operating at elevated temperature have higher drive current and transconductance, less short channel effect, and better subthreshold characteristics than partially depleted SOI MOSFETs.

Ⅰ. Introduction

SOI DTMOS devices have been receiving a lot of attention due to their potential for low power and high speed VLSI circuit applications[1]. Recently the rapid growth of potable electronics and wireless communication system increases the demand for DTMOS devices[2,3].

The use of the bulk CMOS in the high temperature range is limited by the latch-up due to the large leakage current through the well junction at elevated temperature. Since a SOI device is free from latch-up, it has been generally accepted that the temperature range of operation could be expended to high temperature (~300℃). As an operating temperature increases, these are the reduction of

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threshold voltage, the increase of leakage current, the decrease of drain current, and the less hot carrier effects due to the reduction of generation by impact ionization.

D. S. Jeon et al. have developed a temperature dependent SOI MOSFET model for high temperature application(27℃~300℃) and G. Groeseneken et al. have described the temperature dependence of threshold voltage in fully depleted SOI MOSFET's[4,5]. It is experimentally observed that the slope in the plot of threshold voltage versus temperature is smaller in fully depleted SOI MOSFET than partially depleted SOI MOSFET. It is also experimentally observed that the leakage of SOI MOSFETs and reverse biased diodes varies as an intrinsic carrier concentration, n_i, below a temperature of 150℃ and as n_i^2 above that temperature. In 2002, T. Rudenko et al. have reported that at high temperatures the depletion appro- ximation and the charge sheet model are no longer applicable, and thus the classical expression for the subthreshold slope is incorrect for both thin-film FD and thick-film PD devices[6]. Even though T. Douseki et al. have reported that MTCMOS circuits offered the advantage of less variation in leakage current and delay time over a wide temperature range(-25℃~125℃), there is no rigorous study on temperature effects in DTMOS devices[7].

Ⅱ. Experimental

The DTMOS structure used in this work is partially depleted, enhancement mode n-channel MOSFETs fabricated using a standard SOI CMOS process on a SIMOX substrate. The buried oxide thickness, the silicon film thickness and the gate oxide thickness are 400㎚, 8㎚ and 80㎚ respectively. The transistor body is tied to the gate via an aluminum interconnect and the channel doping concentration is about $9 \times 10^{16} cm^{-3}$. Conventional partially deplet-ed(PD) MOSFETs with the same structural and technological parameters as DTMOS are fabricated on the same chip as the DTMOS devices and the channel length and width of the devices are 0.3㎛ and 10㎛, respectively. Measurements of drain current versus gate and drain voltage characteristics have been performed on a temperature-regulated hot chuck at diff- erent drain and gate biases in the range of 25℃~150℃. The substrate of PD MOSFET was kept floating during all measurements.

Ⅲ. Results and discussion

Fig. 1 shows the drain current of a DTMOS device, the drain current of the associated PD MOSFET, and the collector current of the associated n-p-n bipolar transistor at 25℃ and 100℃. The measurement gate voltage is 0.6V and 9V. The drain current of DTMOS device is about 2.5 times that of PD MOSFET at V_{GS} =0.6V and 1.5 times at V_{GS} =0.9V at 25℃. The drain current of DTMOS device and PD MOSFET increase with temperature at V_{GS} =0.6V. However, it is observed that the drain current of both devices is decreased with temperature at V_{GS} =0.9V. The bipolar

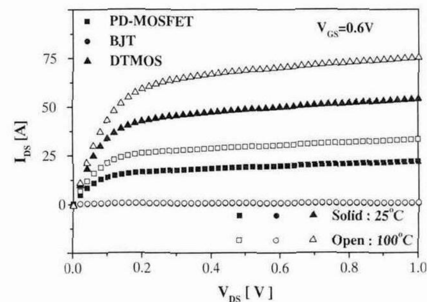

Fig. 1-a. Drain current characteristics at $V_{GS} = 0.6V$ with temperatures of 25℃(solid) and 100℃(open)

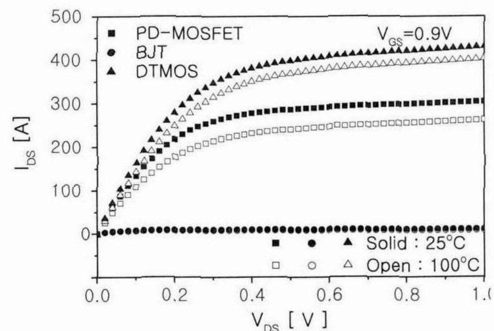

Fig. 1-b. Drain current characteristic at $V_{GS} = 0.9V$ with temperatures of 25℃(solid) and 100℃(open)

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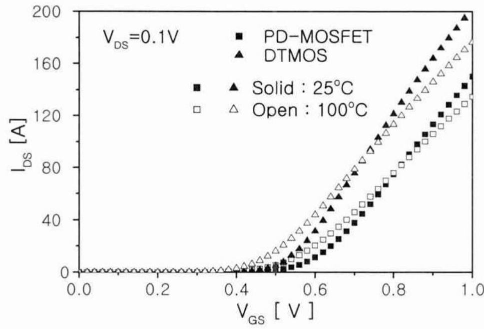

Fig. 2. Drain current versus gate voltage of PD MOSFET and DTMOS device at 25℃(solid) and 100℃(open)

current, I_{BJT}, is much smaller than I_{MOS} and I_X. Since I_{BJT} is very small compared to I_{MOS} and I_X at V_{GS}=0.6V, i.e. when the gate(body) voltage is lower than the built-in potential of source-body junction, we believe that the dominant current in the DTMOS devices at low gate voltage is I_X. Comparing the drain current at V_{GS}=0.6V with that at V_{GS}=0.9V(Fig. 1), one observes that the dependence of the drain current in the DTMOS device on gate voltage is the same as that the PD MOSFET.

Fig. 2 shows the drain current versus gate voltage of PD MOSFET and DTMOS devices at 25℃ and 100℃. The measurement drain voltage is 0.1V. The drain current in both the PD MOSFET and the DTMOS increases with at elevated temperature below the zero - temperature - coefficient(ZTC) point and it decreases above it. The increase of current with temperature increase below the ZTC point is due to the reduction of threshold voltage and the increase of diffusion currents, while above the ZTC point the current decrease is due to the reduction of mobility with temperature.

Fig. 3 shows the temperature dependence of I_X versus gate voltage at V_{DS}=0.1V and V_{DS}=1.0V. The temperature dependence of I_X is very similar to the temperature dependence of channel current in PD MOSFETs. I_X increases with operating temperature below ZTC point due to the increase of electron injection from the source to

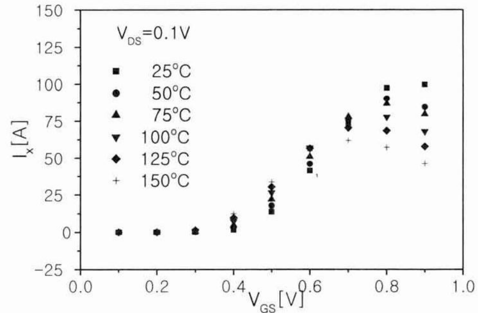

Fig. 3-a. Temperature dependence of I_X versus gate voltage at V_{DS}=0.1V

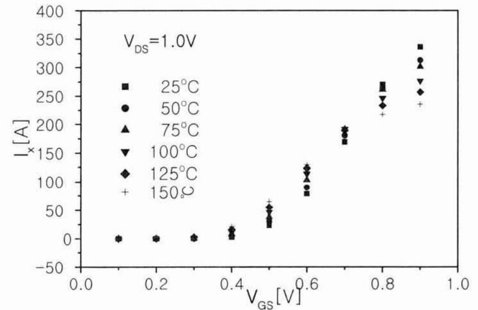

Fig. 3-b. Temperature dependence of I_X versus gate voltage at V_{DS}=1.0V

the channel region. However, I_X decrease with operating temperature above ZTC point due to the reduction of electron mobility in the channel region. The temperature dependence of I_X proves that the physical mechanism of I_X can be explained by the electron injection from the source through the BIBL effect toward the channel region by the gate-related electric field.

Fig. 4 shows the transconductance(gm) versus the gate voltage characteristics of PD MOSFET and DTMOS devices at different temperatures measured at a drain voltage of 0.1V. In the PD MOSFET, gm increases with increased temperature below the ZTC point due to a reduction of threshold voltage and it decreases above ZTC due to the reduction of mobility. The shift of the maximum value of gm to the left is roughly equal to the decrease in threshold voltage. In the DTMOS devices, gm also increases with temperature at low gate voltage and decreases at

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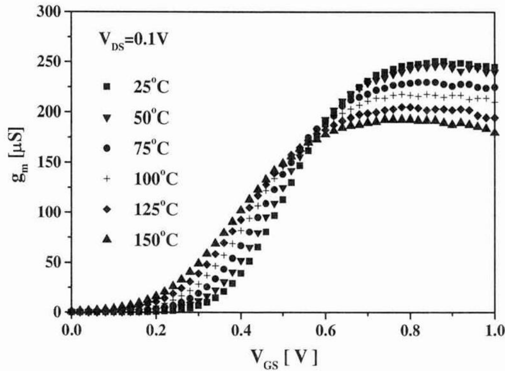

Fig. 4-a. Transconductance versus gate voltage characteristics of PD MOSFETs

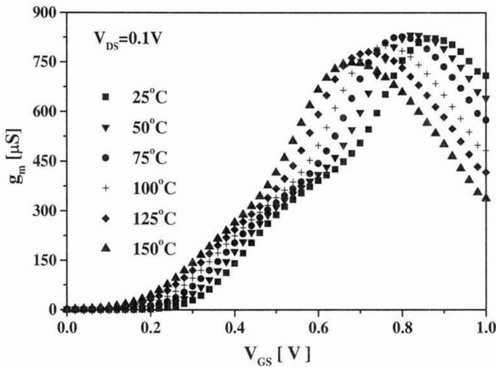

Fig. 4-b. Transconductance versus gate voltage characteristics of DTMOS devices

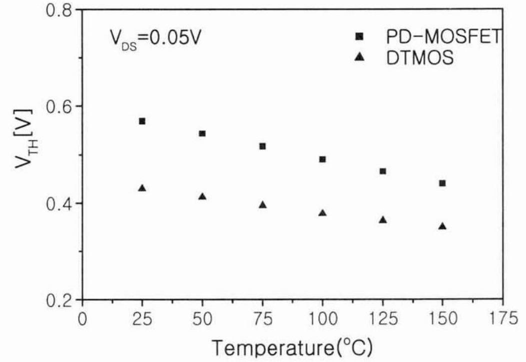

Fig. 5. Temperature dependence of threshold voltage of PD MOSFETs and DTMOS devices

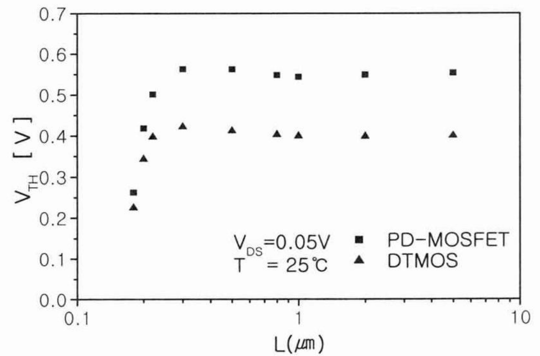

Fig. 6. Threshold voltage as a function of gate length in PD MOSFETs and DTMOS devices

high gate voltage. However, the shift of maximum gm toward lower gate voltages is larger than the threshold shift with temperature. Furthermore, the reduction of the maximum gm when the temperature is increased from 25℃ to 150℃ is only 12%, compared to 30% in the PDSOI device.

Therefore, we conclude that the lower reduction of maximum gm with temperature is due to the reduction of built-in potential of source-body junction with temperature, which increases the I_X current component and, hence, the transconductance. Fig. 5 shows the experimental data for the temperature dependence of the threshold voltage in our PD MOSFETs and DTMOS devices. The measurement drain voltage is 0.05V and the threshold voltage is defined as the gate voltage necessary to reach a drain current of 0.1(W/L)μA. The measured value for dV_T/dT is approximately -1.0mV/K in PD MOSFETs and -0.7 mV/K in DTMOS devices. From the theoretical model and the experimentally measured data, the temperature dependent behavior of threshold voltage in DTMOS devices looks like to that of FD SOI MOSFET.

Fig. 6 shows the threshold voltage as a function of gate length in PD MOSFET and DTMOS devices. The smaller roll-off effect reported in DTMOS devices can be explained by the reduction of depletion charge controlled by the source and drain. Because of the forward bias at source-body junction and the lower reverse bias at drain-body junction (V_D-V_G instead of V_D in a regular SOI MOSFET), the charge controlled by the source and drain decreases and thus leads to the increase of the effective electrical channel length.

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Fig. 7 shows the threshold voltage as a function of gate length at 100℃. From measured data of threshold voltage as a function of gate length at high operating temperature, the absolute roll-off value of threshold voltage between the long channel and the short channel does not depend on the temperature. For short channel MOSFET, and due to the proximity of the source and drain, the

threshold voltage is affected by the source-drain bias, especially at high values of drain voltage. The drain region can be thought of as a second gate causing the channel length modulation and lowering the potential barrier near the source. The drain-induced barrier lowering effect(DIBL) is also due to variation of charge sharing between the gate and the junctions with drain voltage.

Fig. 8 shows the comparison of subthreshold characteristics between DTMOS device and PD MOSFET at V_{DS}=0.1V. Because of a better control of the depletion charge in the channel, DTMOS devices have better subthreshold characteristics than PD MOSFETs. One important device characteristic in the subthreshold regime is the slope of log I_{DS} versus V_{GS}. This characteristic indicates how effectively a MOSFET can be turned OFF as V_{GS} is decreased below threshold voltage. The inverse of the slope is defined as the subthreshold swing. Fig. 9 shows the subthreshold swing as a function of gate length in PD MOSFET and DTMOS devices. It can be observed that the subthreshold swing of DTMOS devices is nearly equal to an ideal value of 60㎷/decade for gate lengths above 0.4㎛. The fact that DTMOS devices have an ideal subthreshold swing indicates that any increase of gate bias V_{GS} will give rise to an identical increase of surface potential Φ_S equal to V_{GS} and, therefore, a perfect coupling between V_{GS} and Φ_S.

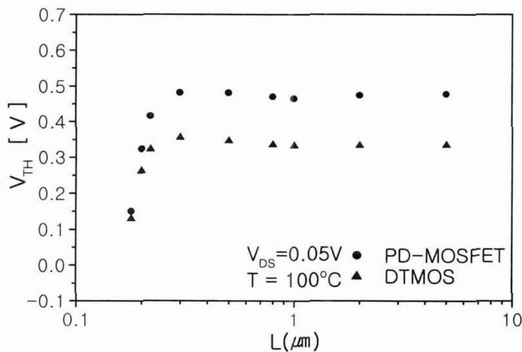

Fig. 7. threshold voltage as a function of gate length at 100℃

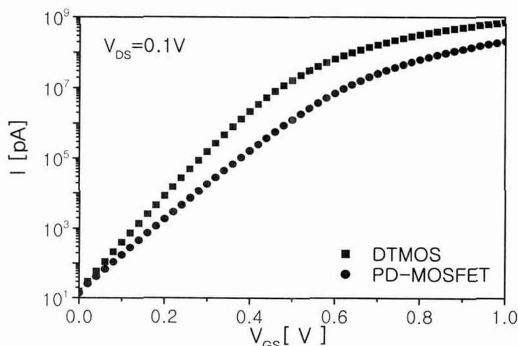

Fig. 8. Comparison of subthreshold characteristics between DTMOS device and PD MOSFET at V_{DS}=0.1V

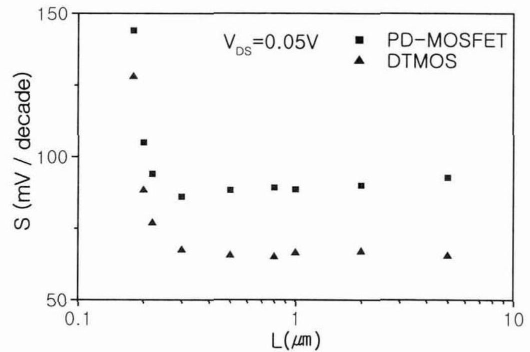

Fig. 9. Subthreshold swing as a function of gate length in PD MOSFETs and DTMOS devices

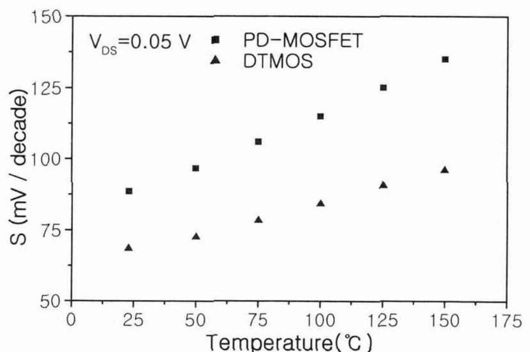

Fig. 10. Subthreshold swing as a function of temperature in PD MOSFETs and DTMOS devices

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Fig. 10 shows the temperature dependence of the subthreshold swing in PD MOSFETs and DTMOS devices. The subthreshold swing of DTMOS devices is less dependent on the temperature than that of PD MOSFET. In the case of a PD MOSFET the depletion capacitance increases with temperature due to the reduction of surface potential with temperature while the surface potential does not depend on the depletion capacitance in DTMOS devices.

Ⅳ. Conclusion

In this paper, we report the temperature dependence of the characteristics of short-channel DTMOS devices and compares them to those of "regular" partially depleted(PD) SOI MOSFETs. Also, the characteristics of SOI DTMOS transistors are experimentally investigated at various temperatures and compared with those of partially depleted SOI MOSFET. The measured characteristics are explained in terms of charge-sharing between the gate and the source/drain junctions. From the comparison with partially depleted SOI MOSFET, it is observed that DTMOS devices operating at elevated temperature have higher drive current and transconductance, less short channel effect, and better subthreshold characteristics than partially depleted SOI MOSFETs. Therefore, DTMOS devices have better characteristics than their PDSOI counterparts, which renders them very attractive for low-voltage CMOS applications.

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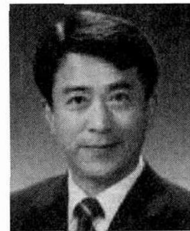

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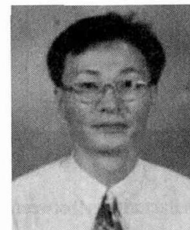

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