An Efficient Code Acquisition Scheme for DSSS-based Real-Time Locating Systems

Jongtae Lim*, Hyung-Rae Park** *Regular Members*

ABSTRACT

This paper proposes an efficient code acquisition scheme for direct-sequence spread spectrum (DSSS) based real-time locating systems (RTLS). The proposed scheme employs multiple bit integration to significantly decrease false alarms when no packet signal is transmitted and increase the detection probability when the RTLS tags are excited. The performance of the proposed code acquisition scheme is analyzed and numerically evaluated, and compared with those of single-dwell and traditional double-dwell code acquisition schemes. The simulation results show that the proposed multiple-bit integration scheme outperforms single-dwell and double-dwell schemes.

Key Words : Real-Time Locating Systems, Code Acquisition, Direct Sequence Spread Spectrum, RFID

Ⅰ. Introduction

In radio-frequency identification (RFID) applications, real-time locating systems (RTLS) have recently emerged as fully-automated wireless systems that continually monitor the locations of an item[1]. Shipment tracking and tracing may be a common example of RFID-based RTLS applications in the industrial RTLS market. To configure RTLS systems, we need RTLS transmitters, i.e. active RFID tags whose behavior is altered by RTLS exciter, RTLS readers that receive information packets from RTLS transmitters, and RTLS servers that aggregate data from the readers and determines location of transmitters.

In designing RTLS systems many wireless communication functionalities such as noncoherent demodulation scheme, automatic gain control, code acquisition and tracking, and automatic frequency control need to be devised for RTLS readers. Especially, the initial code acquisition is one of the most essential parts for determining the system performance. Many code acquisition systems such as single-dwell and double-dwell scheme have been developed and widely used for accurate and rapid acquisition in direct-sequence code-division multiple-access (DS-CDMA) systems[2-4]. However, those schemes need the further performance improvements applied directly to RTLS systems due to some characteristics of the RTLS system environment. The purpose of this paper is to develop an efficient code acquisition scheme for RTLS systems, that improves the acquisition performance instead of employing the conventional single-dwell and double-dwell schemes based on DS-CDMA systems.

RTLS systems have to continually perform the initial code acquisition since the RTLS reader cannot figure out the time that the RTLS transmitter sends a packet or the RTLS exciter triggers the transmitters. Also, various synchronization procedures such as code acquisition, code tracking, and automatic frequency control (AFC) should be performed within the 8-symbol preamble period and

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the length of RTLS message packet is very short, being less than a few milliseconds[1]. Thus, unlike DS-CDMA systems in which the base station knows a mobile's access time interval and the packet is long, RTLS systems need to have significantly small false alarm probability, especially when no packet signal is transmitted. If the probability is not sufficiently small, the reader has high chance of declaring a false alarm and takes some recovery time to be ready for another acquisition procedure. Thus, the reader cannot detect the packet sent by the transmitter triggered during the recovery time.

In this paper, we propose an efficient code acquisition scheme using multiple bit integration to significantly decrease false alarms when no packet signal is transmitted and simultaneously increase the detection probability when the RTLS transmitters send the packet signals. The RTLS systems considered in this paper are fully compatible with the 2.4 GHz systems defined in the international standard, ISO/IEC 24730. The probabilities of detection and false alarms of the proposed multiple-bit integration code acquisition schemes as well as single-dwell and multiple-dwell schemes are analytically derived and numerically evaluated to verify the validity of the proposed acquisition scheme for RTLS systems.

The remaining parts of the paper are organized as follows. Section II provides RTLS system description and the code acquisition schemes. The performance analysis of the code acquisition schemes are given in Section III, and the numerical results are presented in Section IV. Finally, we conclude this paper in Section V.

II. RTLS Systems and Code Acquisition

This section gives brief description of RTLS system architecture and detailed information of the proposed code acquisition scheme as well as the conventional single-dwell and double-dwell schemes.

2.1 RTLS System Description

Fig. 1 shows the basic elements of RTLS infrastructure[1] that consists of an exciter, RTLS
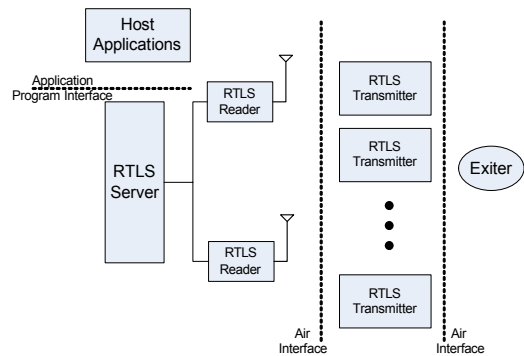

Fig. 1. Basic elements of RTLS infrastructure

transmitters, an RTLS server, RTLS readers and host applications. The exciter is a device that transmits a signal that alters the behavior of the RTLS transmitters. The RTLS transmitters are the battery powered radio devices that are attached to assets or items and transmit the message packet signals that provide the unique transmitter ID and certain status information about the transmitter and items.

The RTLS readers receive the signals from the RTLS transmitters and demodulate the Direct Sequence Spread Spectrum (DSSS) signals. The RTLS server is a computing device that aggregates data from the readers and determines the location of the transmitters. The server is managed by host application through the application program

Table 1. Main Physical Layer Parameters for RTLS Systems

Parameter Name	Description
Modulation	BPSK DSSS
Data encoding	Differentially encoded
Operating frequency range	2400 MHz - 2483.50 MHz
Center frequency	2441.750 MHz
Operating frequency accuracy	±25 ppm maximum
Occupied channel bandwidth	60 MHz
Data bit rate	59.7 kb/s
PN chip rate	30.521875MHz ±25 ppm
PN code length	511
Data packet lengths	56, 72, 88, 152 bits

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interface.

The wireless communication protocol between the transmitter and readers is well defined in the international standard, ISO/IEC 24730-2[1]. The system operates in the 2400 MHz to 2483.50 MHz frequencies and employs Binary Phase Shift Keying (BPSK) DSSS modulation that requires pseudo-noise (PN) sequences of the local generator. The main physical layer parameters for the RTLS systems are summarized in Table I.

2.2 Code Acquisition

To demodulate the received packet signals at the DSSS-based RTLS reader, various synchronization procedures such as code acquisition, code tracking and automatic frequency control (AFC) should be performed within the 8-symbol preamble period. Since the 8-symbol preamble period is not enough to process the synchronization procedures, the preamble period needs to be carefully partitioned into the sub-periods performing each synchronization procedure. One example of the preamble partition is shown in Fig. 2.

The synchronization procedures start with the PN code sequence synchronization which synchronizes PN sequences of the local generator at the reader and the received signals within a small fraction of one PN chip. The PN code synchronization consists of two steps: code and code tracking. In the code acquisition step, the initial code phase is determined and the PN sequence code phase synchronization is maintained through the code tracking procedure.

In general, for the initial code acquisition, the PN reference sequences of the local generator are correlated with the received signal and then the outputs are accumulated to form a decision variable. By advancing the position of the code sequence, the decision variables are calculated for the different code phases. If the decision variables for the selected number of the test cell positions are obtained, the decision is made as to the acquisition success or failure. If the maximum value of the decision variables is greater than a given threshold, the system assumes the code sequence is in-phase at the position. Otherwise, another code acquisition procedure is performed.

Single-dwell code acquisition scheme utilizes the received signal data corresponding to one-bit symbol. The performance of single-dwell code acquisition scheme depends on the choice of the threshold and the number of the accumulated PN chips. To improve the detection performance, double-dwell scheme is used, which consists of two steps: initial search and verification step. In the initial search step, the same procedure as single-dwell scheme is performed. In the verification step, the decision variable for the cell position obtained in the initial search step is evaluated for the next data bit symbol. If the statistic is also greater than the threshold, then the cell is assumed to be in-phase at the cell position. Double-dwell scheme definitely improves the detection probability compared with single-dwell scheme. However, double-dwell scheme degrades the false alarm performance when the packet signal is not transmitted. The detailed performance of single-dwell and double-dwell schemes is dealt with in the subsequent sections. As said earlier, the false alarm performance is the most significant factor for RTLS system performance.

To overcome this degradation and improve the detection performance further, we consider multiple-bit integration code acquisition scheme shown in Fig. 3. In the proposed code acquisition scheme, decision variables are calculated using N_b-bit symbols. Since the PN code length of RTLS systems is 511, if the search step size is selected as the half of the chip duration, then 2x511 decision variables are to be evaluated for N_b-bit data symbols
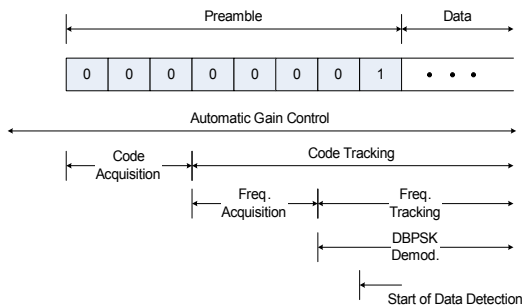

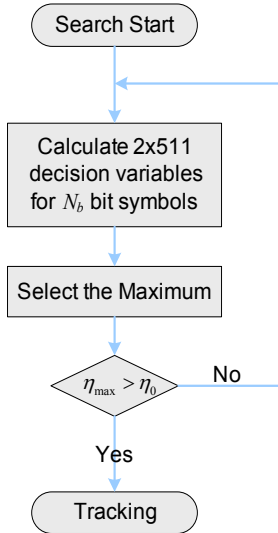Fig. 2. Example of the preamble partition for the RTLS reader

Fig. 3. Multiple-bit integration code acquisition algorithm

in the scheme. If the maximum of the variables, is greater η_{max} than the decision threshold, η_0 the system assumes the cell is in-phase and then the code tracking procedure is performed. Otherwise, the system repeats the code acquisition step. We note that single-dwell scheme is corresponding to multiple-bit integration code acquisition scheme with $N_b = 1$. For the implementation of the multiple-bit integration code acquisition scheme, we employ matched filter architecture shown in Fig. 4. Considering the large frequency offset error up to ±25 ppm (60 kHz), sub-bit correlation processing is used and thus we select the search step size as the half of the chip duration. Then 2x511 test cell positions are evaluated. Since the processing gain decreases as the number of the accumulated PN chips gets smaller, the accumulation length is selected to the appropriate value. It can be seen that
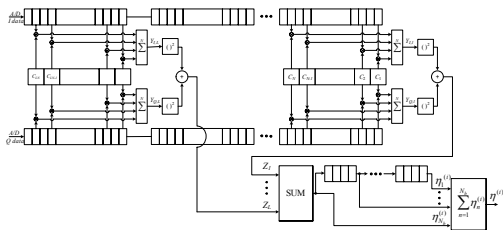

Fig. 4. Matched filter architecture for initial code acquisition

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the energy loss for the frequency offset is [2]

$$D(\Delta f) \approx \left[\sin(\pi N \Delta f T_c) / (\pi N \Delta f T) \right]^2 , \qquad (1)$$

where N is the accumulation length, Δf is the frequency offset, and T_c is the chip duration. For the maximum frequency offset for RTLS systems, 60 kHz, the energy loss is 0.22 dB, 0.9 dB, and 3.92 dB for N = 64, 128, and 256, respectively. Thus, we select the accumulation length as 128. The 2x511 I/Q data that are sampled with $0.5T_c$ period are fed into data buffer. The buffer contains the data corresponding to one-bit symbol.Since the accumulation length is 128, the buffered data are divided into 4 groups. For each group the I/Q accumulator outputs are squared and summed. The sum of 4 statistics are added together to give a decision variable for the given data symbol. The decision variables for N_b symbolbits are obtained by the same way and added to give the final decision variable. As shown in Fig. 4, the proposed algorithm does not require addition hardware except the delay buffer of decision variable for one symbol bit compared with single-dwell scheme. Thus, the complexity of the proposed scheme is nearly same as that of single-dwell scheme.

Ⅲ. Performance Analysis

The PN code acquisition can be considered as a binary hypothesis testing problem with the null hypothesis H_0 and the alternative hypothesis H_1:

$$\begin{aligned} H_0 &: |\tau| > T_c \\ H_1 &: |\tau| \le T_c, \end{aligned} \qquad (2)$$

where, τ is the timing error. H_1 is the hypothesis that the received signal and the local PN code sequence are aligned within one PN chip[2]. For many open-field RTLS applications such as container shipment tracking and tracing, we can assume line-of-sight transmission and thus an additive white Guassian noise (AWGN) channel

environment[1]. For an AWGN channel The lth accumulator output for the ith H_1 cell is given as [5]

$$Y_{I,l} = N\sqrt{E_C}R(\tau_i)\cos\varphi + n_I$$
$$Y_{Q,l} = N\sqrt{E_C}R(\tau_i)\sin\varphi + n_Q, \quad (3)$$

where N is the number of accumulated PN chips, E_C is the signal energy per chip, t_i is the timing error for the ith H_1 cell, j is the phase of signal, and $R(t)$ is the convolution of the impulse response of a pulse-shaping filter with that of the matched filter. The I/Q channel noise components n_I and n_Q are assumed to be Gaussian with a variance of $(NN_0)/2$, where N_0 is the power spectral density due to the noises. Thus, the accumulator outputs, have Gaussian distributions $Y_{I,l}$, $Y_{Q,l}$ with the variance $(NN_0)/2$ and the means $N\sqrt{E_c}R(\tau_i)\cos\phi$, $N\sqrt{E_c}R(\tau_i)\sin\phi$ respectively. Thus, under H_1 where the timing error is within one chip, $R(t)$ is greater than zero, the squared sum of the accumulator outputs, $Z_l = Y_{I,l}^2 + Y_{Q,l}^2$ becomes a noncentral chi-squared random variable with two degrees of freedom. The decision variable for the ith cell position of the nth symbol data, $\eta_n^{(i)}$ is given by

$$\eta_n^{(i)} = \sum_{l=1}^{L} Z_l = \sum_{l=1}^{L}\left(Y_{I,l}^2 + Y_{Q,l}^2\right) \quad (4)$$

where, L is the number of accumulation groups for the data corresponding to one symbol and becomes 4 in our selection. And the final decision variable in the proposed multiple-bit integration scheme $\eta^{(i)}$ is given by

$$\eta^{(i)} = \sum_{n=1}^{N_b} \eta_n^{(i)} \quad (5)$$

and thus $\eta^{(i)}$ is a noncentral chi-squared random variable with $2LN_b$ degrees of freedom whose probability density function (p.d.f.) is

$$f_{\eta_i}(\eta_i \mid H_1) = 1/V_n\left(\eta_i/s_i^2\right)^{(N_bL-1)/2}$$
$$\cdot \exp\left(-(\eta_i + s_i^2)/V_n\right)I_{N_bL-1}\left(2\sqrt{\eta_i s_i^2}/V_n\right), \quad (6)$$

where, $I_{N_bL-1}(x)$ is the $(N_bL-1)^{th}$ order modified Bessel function of the first kind, $V_n = NN_0$ and $s_i^2 = N_bLN^2E_CR^2(\tau)$. Also, under H_0, $R(t)$ is nearly zero and thus the p.d.f. of the decision variable under H_0 is

$$f_\eta(\eta \mid H_0) = 1/\left((N_bL-1)!V_n^{N_bL}\right)\eta^{N_bL-1}\exp(-\eta/V_n). \quad (7)$$

To derive the detection and false-alarm probabilities, we first consider the case that any packet signal is not present in the search window, i.e., no RTLS transmitters are active. In this case, the probability of false alarm is

$$P_F^{(0)} = 1 - \left[\int_0^{\eta_0} f_\eta(\eta \mid H_0)d\eta\right]^{N_t}$$
$$= 1 - \left(1 - \exp(-\eta_0/V_n)\sum_{k=0}^{N_bL-1} 1/(k!)(\eta_0/V_n)^k\right)^{N_t}, \quad (9)$$

where, N_t is the number of test cell positions.

Next, we consider the case that a packet signal is present in the search window. We assume that there are N_{H_i} H_1 cells. The probability that the decision variable of the ith H_1 cell is the greatest among all the test cells and greater than the threshold is given by

$$P_{D,i} = \int_{\eta_0}^{\infty}\left(\int_0^{\eta_i} f_\eta(\eta \mid H_0)d\eta\right)^{N_t-N_{H_1}}$$
$$\cdot \prod_{\substack{j=1\\j\neq i}}^{N_{H_1}}\left(\int_0^{\eta_i} f_{\eta_j}(\eta_j \mid H_1)d\eta_j\right)\cdot f_{\eta_i}(\eta_i \mid H_1)d\eta_i$$
$$= \int_{\eta_0}^{\infty}\left(1 - \exp(-\eta_i/V_n)\sum_{k=0}^{N_bL-1} 1/(k!)(\eta_i/V_n)^k\right)^{N_t-N_{H_1}} \quad (10)$$
$$\cdot \prod_{\substack{j=1\\j\neq i}}^{N_{H_1}}\left(1 - Q_{N_bL}\left(\sqrt{2s_j^2/V_n}, \sqrt{2\eta_i/V_n}\right)\right)f_{\eta_i}(\eta_i \mid H_1)d\eta_i,$$

where $Q_{N_bL}(x)$ is the generalized Marcum's Q function. Since there are N_{H_i} H_1 cells, the probability of detection is

$$P_D = \sum_{i=1}^{N_{H_1}} P_{D,i}. \quad (11)$$

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The probability of miss is

$$P_M = \left(\int_0^{\eta_0} f_\eta(\eta \mid H_0)d\eta\right)^{N_t-N_{H_1}} \cdot \prod_{j=1}^{N_{H_1}}\int_0^{\eta_0} f_{\eta_j}(\eta_j \mid H_1)d\eta_j$$

$$= \left(1-\exp(-\eta_i/V_n)\sum_{k=0}^{N_bL-1}1/(k!)(\eta_i/V_n)^k\right)^{N_t-N_{H_1}} \quad (12)$$

$$\cdot \prod_{j=1}^{N_{H_1}}\left(1-Q_{N_bL}\left(\sqrt{2s_j^2/V_n},\sqrt{2\eta_0/V_n}\right)\right).$$

The probability of false alarm is given by

$$P_F = 1 - P_D - P_M. \quad (13)$$

As stated in the previous section, since the single-dwell scheme is corresponding to a multiple-bit integration scheme with N_b = 1, the probabilities for the single-dwell scheme are obtained by setting N_b as 1 in the above equations.

For the double-dwell scheme, when the packet signal is presented in the search window, the probability of detection is given by

$$P_D = \sum_{i=1}^{N_{H_1}}P_{D,i}^{(1)}\int_{\eta_0}^\infty f_{\eta_i}(\eta_i \mid H_1)d\eta_i$$

$$= \sum_{i=1}^{N_{H_1}}P_{D,i}^{(1)}\ Q_L\left(\sqrt{2s_i^2/V_n},\sqrt{2\eta_0/V_n}\right), \quad (14)$$

where $P_{D,i}^{(1)}$ is the probability given by (10) with N_b = 1, Also, the probability of false alarm when no signal is present in the search window is

$$P_F = \sum_{i=1}^{N_t}P_{F,i}^{(1)}\int_{\eta_0}^\infty f_\eta(\eta \mid H_0)d\eta$$

$$= \sum_{i=1}^{N_t}P_{F,i}^{(1)}\left(\exp(-\eta_0/V_n)\sum_{k=0}^{L-1}1/(k!)(\eta_0/V_n)^k\right), \quad (15)$$

where $P_{F,i}^{(1)}$ is the probability that the decision variable for the ith cell is the largest among all the test cells and greater than the decision threshold for the initial search step of double-dwell scheme, and is given by

$$P_{F,i}^{(1)} = \int_{\eta_0}^\infty\left(\int_0^{\eta_i} f_\eta(\eta \mid H_0)d\eta\right)^{N_t-1} f_\eta(\eta_i \mid H_0)d\eta_i. \quad (16)$$

Ⅳ. Numerical Results

We performed numerical evaluation of the probabilities of detection and false alarm for single-dwell scheme, double-dwell scheme, and the proposed multiple-bit integration code acquisition scheme. The calculation is performed for the search step size of 1/2 PN chip. For the convenience we used 512 PN code length and thus the decision statistics of total N_t = 1024 test cell positions are evaluated. And the number of H_1 cells, N_{H_i} is assumed to be 4 and the timing errors are selected as $\pm 1/4T_c$ and $\pm 3/4T_c$ to reflect the worst misalignment under H_1 .

Fig. 5 shows the probabilities of false alarm for single-dwell scheme, double-dwell scheme, and multiple-bit integration scheme with 2-bit and 3-bit integration when no packet signal is present in the search window. The probabilities are evaluated at the nominal target SNR, 15 dB and the decision thresholds are chosen to give the probability of false alarm of 10^{-4}. The selected decision thresholds are 24, 14.4, 32.2, and 39.4 for single-dwell, double-dwell, 2-bit integration, and 3-bit integration scheme, respectively.

To figure out the detection performance, we plotted the detection probabilities for each scheme in Fig. 6. For a fixed SNR, the detection probability of the proposed multiple-bit integration scheme is higher than those of single-dwell and double-dwell scheme. We can choose the primary performance metric as the required SNR at which the probability of detection is greater or equal to 0.9. The required SNR's for the performance metric are 15.1, 14, 12.8, and 11.6 dB for single-dwell, double-dwell scheme, and the multiple-bit integration scheme with 2-bit and 3-bit integration, respectively. Thus, the multiple-bit integration code acquisition scheme outperforms the traditional single-dwell and double-dwell scheme. To further improve the performance of the multiple-bit integration scheme, the number of integrated bits should be larger. However, the number is limited by the preamble size of the RTLS packet. Considering the 8-bit
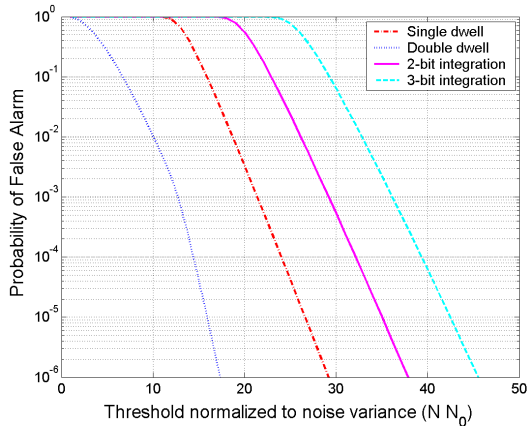
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Fig. 5. Probability of false alarm for single-dwell, double-dwell, 2-bit integration and 3-bit integration scheme for the target SNR, 15dB
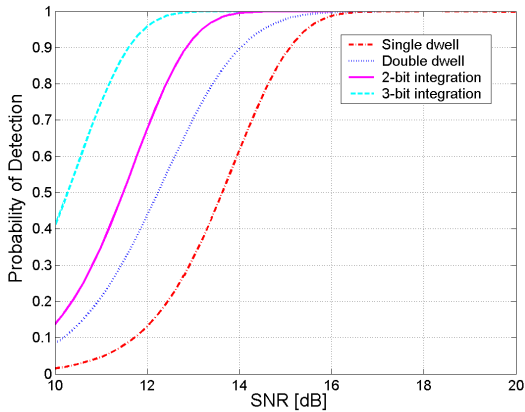

Fig. 6. Detection probability for single-dwell, double-dwell, 2-bit integration and 3-bit integration scheme in AWGN with $P_F^{(0)} = 10^{-4}$

preamble size of RTLS systems, we can select 2-bit integration scheme.

V. Conclusion

In this paper, we proposed a multiple-bit integration code acquisition scheme for the initial PN code synchronization for DSSS-based RTLS systems. The expressions for the probabilities of detection and false alarm are derived and the numerical evaluation is performed. The numerical evaluation shows that the proposed scheme provides better detection performance than the traditional single-dwell and double-dwell scheme. Especially,

the proposed matched-filter architecture does not increase the hardware complexity and thus single-dwell architecture can be used with the added buffer for decision variables.

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Jongtae Lim   Regular Member

Jongtae Lim received the B.S. (summa cum laude) and M.S. degrees in Electronics Engineering from Seoul National University, Seoul, Korea in 1989 and 1991, respectively, and received the Ph.D. degree from the Department of Electrical Engineering and Computer Science, University of Michigan, AnnArbor, in 2001. In Sep. 2004, he joined Korea Aerospace University, Goyang, Korea. Since March 2008, he has been with Hongik University, Seoul, Korea, where he is now Associate Professor of the School of Electronic & Electrical Engineering. His research and teaching interest are in digital communications, broadcasting systems and signal processing.

Hyung-Rae Park   Regular Member

Hyung-Rae Park (M'94) received the B.S. degree from Korea Aerospace University, Korea in 1982, the M.S. degree from Yonsei University, Seoul, Korea in 1985 and the Ph.D. degree from Syracuse University, Syracuse, NY in 1993, all in electrical engineering. From 1985 to 1999, he was with ETRI, Korea, as a Section Head in the Mobile Communication Research Division. From 1999 to 2000, he was a Vice President of C&S Technology, Inc., Korea. Since 2001, he has been a Faculty Member with the School of Electronics, Telecommunications, and Computer Engineering, Korea Aerospace University. His research interests include code-division multiple-access algorithm development and MODEM design, orthogonal frequency-division multiplexing system design, array signal processing for communications, and radar signal processing.