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광역 WPAN 응용을 위한 주파수 오차에 강인한 최적 다중비트 디지털 FSK 수신기

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An Optimized Multi-Bit Digital FSK Receiver Robust to CFO for Long-Range WPAN Applications

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요 약

본 논문은 최근 표준화가 진행 중인 광역 WPAN에서 주파수 옵셋에 강인한 최적화된 다중 비트 기반 디지털 FSK 수신기에 대해서 제안한다. 광역 WPAN FSK 표준에서는 기존보다 짧은 프리앰블을 사용하고 있으며, 통신 반경이 늘어남에 따라 엄격한 BER 요구사항을 제시하고 있다. 이러한 요구사항을 만족하기 위해서 본 논문에서는 CFO가 있는 상황에서도 간단하면서 BER 성능을 만족할 수 있는 최적화된 디지털 FSK 수신기를 설계하였다. 시뮬레이션을 통해 광역 WPAN FSK 시스템에서 필요한 비트 수를 결정하고, 짧은 프리앰블을 사용함에도 CFO에 상관없이 요구 BER 성능을 만족시킬 수 있음을 증명하여 제안된 FSK 수신기가 최근 광역 WPAN 응용에 적절함을 보였다.

Key Words : WPAN, FSK, digital receiver, frequency offset

ABSTRACT

This paper proposes an optimized multi-bit digital FSK receiver robust to large carrier frequency offset (CFO) toward recently emerging long-range WPAN standards. Due to a short preamble length and strict BER requirements, we design a simple multi-bit digital demodulator combined with CFO estimator which guarantees the target BER performance. Simulation results verify that the proposed FSK receiver achieves CFO-free BER performance with the short preamble and satisfies the BER requirement by the recent WPAN applications.

Ⅰ. Introduction

Recently, there has been a significant interest regarding the optimal command and control applications for smart utility networks (SUN), low energy critical infrastructure monitoring (LECIM) networks, and TV white space (TVWS) WPAN systems[1]. Targeting those applications, the IEEE 802.15 WPAN group has completed 15.4g SUN standard and is currently pursuing standardization of 15.4k LECIM and 15.4m TVWS WPAN. These are commonly developing low-rate wireless connectivity

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with limited battery consumption, typically operating in the long-range, e. g., 1 Km[2].

Accordingly, 15.4g SUN selected the narrow-band FSK PHY and the other 15.4k and 15.4m standards are also considering the similar FSK PHY due to its advantages of low-complexity and low-power consumption[1]. However, those standards demand longer communication range (e. g., 1 Km) and specify the short preamble (e. g., 4-byte), which leads to reconsideration of the existing FSK architectures.

Most conventional approaches toward FSK systems, such as short-range Bluetooth and WBAN, have considered low-cost 1-bit quantization because the limited bit error rate (BER) performance with 1-bit can meet those system requirements[3,4,6]. In addition, the carrier frequency offset (CFO) was conventionally compensated by PLL adjustment or DC offset cancelation for long preamble[4,5]. However, the advent of long-range WPAN applications asks for a judiciously designed FSK receiver to satisfy the strict BER requirement. Moreover, the short preamble requirement for the recent FSK standards makes timing recovery and CFO correction challengeable.

In this paper, we design a multi-bit digital FSK receiver to satisfy the BER and short preamble requirements for recently emerging WPAN standards. First, we introduce the necessity of the multi-bit analog-to-digital converter (ADC) for FSK system. Then, the CFO estimator and demodulator are proposed and optimized with a delay parameter. Based on derived optimization, we also suggest a practical implementation approach for our receiver. Finally, simulation results show that our FSK receiver enjoys CFO-free BER performance with the short preamble, while achieving the target BER.

Ⅱ. Digital FSK Receiver Model

Since we develop a WPAN standard-compliant FSK receiver architecture, let us first consider the link budget of the IEEE 802.15.4g SUN FSK system, where the budget is calculated as 30 dB, as shown in Table 1. Incorporating 10 dB noise figure (NF) for low-cost RF chain, it is required to satisfy the target BER 10^{-5} at SNR 15 dB, including implementation loss and link margin. Since the ideal FSK demodulator requires SNR 13 dB for BER 10^{-5}, a multi-bit ADC is desirable in order to achieve the similar performance with the ideal case.

Figure 1 depicts our FSK receiver architecture equipped with multi-bit ADCs. The first stage of our digital FSK receiver performs CFO estimation and correction to produce the demodulated signal. Then, the second stage conducts clock-data recovery (CDR) and packet recovery which are well-known. In this paper, therefore, we focus on the first stage of Fig. 1.

Due to the strict out-of-band spectral mask specified in WPAN standards, we here consider the continuous-phase FSK signal modulated at the carrier frequency[8]

$$s(t) = \cos[2\pi f_c t + \phi(t;\mathrm{I})], \tag{1}$$

In (1), $\phi(t;\mathrm{I})$ represents the time-varing phase defined as

$$\phi(t;\mathrm{I}) = 4\pi T f_d \int_{-\infty}^{t} [\sum_n I_n g(\tau - nT)] d\tau, \tag{2}$$

where $I_n \in \{\pm 1\}$ denotes the sequence of amplitude obtained by mapping 1-bit information, T

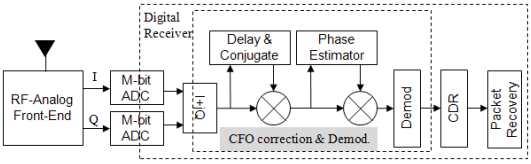

그림 1. 제안된 FSK 수신 구조
Fig. 1. Proposed FSK receiver architecture

표 1. IEEE 802.15.4g SUN FSK 시스템의 Link budget
Table 1. Link budget of IEEE 802.15.4g SUN FSK

Mandatory Data rate	50 Kbps
Channel bandwidth	200 KHz
RX noise level	-121 dBm per channel
Min. receiver sensitivity level	-91 dBm
Budget	30 dB

is a symbol duration, $g(t)$is a rectangular pulse of amplitude of 1/2T and duration T, and $f_d$is the frequency deviation.

At the receiver, the down-mixed signal by f_c -F_{IF} is represented as

$$r(t) = \exp\{j[2\pi(f_{IF} + f_o)t + \phi(t;\mathrm{I})\} + w(t) \qquad (3)$$

where f_O denotes CFO, f_{IF} is an intermediate frequency, the received power is assumed to be unity for simplicity and $w(t)$ is AWGN with $N(0, \sigma^2)$. We note the performance degradation caused by f_o in (3) is a major concern for the WPAN FSK system.

Ⅲ. Digital CFO Correction and Demodulation

Relying on the digital FSK receiver architecture in Fig. 1, we propose to estimate and correct the CFO at every packet reception in digital domain without any information on f_{IF} and f_o. Since the second stage of Fig. 1 works properly after CFO correction, we focus on CFO estimation during preamble, which is multiple repetitions of "10."

The phase of the FSK signal (2) is reversed in every symbol during the preamble. Therefore, the phase difference vector between the received signal and its delayed signal shows a phase transition, which is given by

$$\begin{aligned} c(t;d) &= r(t)\cdot r^*(t-d) \\ &\approx \exp\{j\phi_c + j[\phi(t;\mathrm{I}) - \phi(t-d;\mathrm{I})]\} + \overline{w}(t) \end{aligned} \qquad (4)$$

$\phi_c := 2\pi(f_{IF} + f_o)d$ represents the time- independent constant phase, and $\phi(t;\mathrm{I})$ - $\phi(\mathrm{t}\text{-}d;\mathrm{I})$ denotes the phase difference corresponding to the delay d indicating time-dependent phase transition. The approximate noise term $\overline{w}(t)$ is also AWGN with $N(0,\overline{\sigma}^2)$ where $\overline{\sigma}^2 = 2\sigma^2$.

Assuming $\phi_c = 0$ and $\overline{w}(t) = 0$, the phase of c($t;d$) in the interval of $nT \le t \le (n+1)T$ can be written as

$$\angle c(t;d) = \begin{cases} I_{n-1}\, 2\pi f_d[d - 2(t-nT)], & nT \le t \le nT + d \\ I_n\, 2\pi f_d d, & nT + d \le t \le (n+1)T \end{cases} \qquad (5)$$

where the phase transition occurs in the duration of $nT \le t \le nT + d$.

3.1 CFO Estimation and Correction

Figure 2 demonstrates the complex domain representation of the phase difference vector $c(t;d)$ for both $\phi_c = 0$ and $\phi_c \neq 0$. If $\phi_c = 0$, then we could easily accomplish FSK demodulation of the n th transmitted symbol by comparing the imaginary part of $c(t;d)$, i. e., $\Im[c(t;d)]$ with the decision threshold 0. However, $\phi_c \neq 0$ degrades the BER performance due to shortened decision distance between bit 0 and 1. This motivates acquiring the phase rotation vector $\exp(j\phi_c)$ and compensating it afterwards.

In order to estimate $\exp(j\phi_c)$ from the phase difference vector $c(t;d)$ in (4), we average $c(t;d)$ over multiple $2T$ periods during preamble, which gives the following

$$\eta(t;d) = \frac{1}{2MT}\int_{-MT}^{MT} c(t;d)dt = \exp(j\phi_c)\cdot P(d) + \overline{w}(t) \qquad (6)$$

where M is a non zero integer and $P(d)$ is defined as

$$\begin{aligned} P(d) &= \frac{1}{2MT}\int_{-MT}^{MT} \exp\{j\phi(t;\mathrm{I}) - \phi(t-d;\mathrm{I})\}dt \\ &= \frac{1}{T}[(T-d)\cos(2\pi f_d d) + \frac{1}{\pi f_d}\sin(2\pi f_d d)] \end{aligned} \qquad (7)$$

As in (7), $P(d)$ becomes independent of t due to phase symmetry over $2T$ period, including both 0 → 1 and 1 → 0 transition. We also note that any $2T$ period starting at arbitrary t renders the same $P(d)$. Therefore, $\eta(t;d)$ in (6) can be an estimate of $\exp(j\phi_c)$ thanks to the constant $P(d)$.

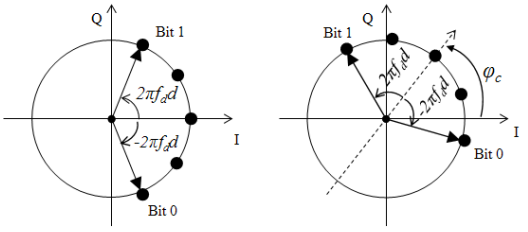

그림 2. c($t;d$)의 복소수 영역 표현: 좌 - $\phi_c = 0$, 우 - $\phi_c \neq 0$
Fig. 2. Complex domain representation of c($t;d$): Left - $\phi_c = 0$, Right - $\phi_c \neq 0$

Since our aim is to compensate the phase rotation vector $\exp(j\phi_c)$ in Fig. 2, $\eta(t;d)$ can be directly used to achieve our CFO-corrected observation $\hat{c}(t;d)$ as

$$\hat{c}(t;d) = c(t;d) \cdot \eta^*(t;d) \tag{8}$$

We notice that our CFO correction in (8) can perform in digital domain without any vector rotation algorithm, e. g., CORDIC.

Now, let us examine identifiability of our CFO estimator $\eta(t;d)$. As shown in (6), averaging $c(t;d)$ over multiple $2T$ duration can estimate the phase rotation vector $\exp(j\phi_c)$ in the range of $0 \le \phi_c \le 2\pi$ without ambiguity, which is the full range. In addition, even though ϕ_c is not within $[0,2\pi)$, $\eta(t;d)$ can still identify the true phase rotation vector determined by $\mathrm{mod}[\phi_c,2\pi]$, where $\mathrm{mod}[\cdot]$ denotes modulo operation. Consequently, our $\eta(t;d)$ can estimate the phase rotation without any limitation on its range.

3.2 Optimization on Delay d

So far, we have estimated the phase rotation vector $\exp(j\phi_c)$ corresponding to the delay d, instead of estimating f_o. Since $P(d)$ in (7) depends on the delay d, we here investigate how to set d for optimal CFO estimation.

Without loss of generality, we assume $f_{IF} = 0$. Then, we can estimate the CFO from (7)

$$\hat{f}_o = \frac{1}{j2\pi d} E\left[\ln\left(\frac{\eta(t;d)}{P(d)}\right)\right] \tag{9}$$

and the CFO error can be defined as

$$\varepsilon = \left|f_o - \hat{f}_o\right| = \frac{1}{2\pi d}\left|\ln\left(1+\frac{\tilde{w}(t)}{\eta(d)}\right)\right| \tag{10}$$

which is approximated at high SNR as following

$$\varepsilon \approx \frac{1}{2\pi d}\left|\frac{\tilde{w}(t)}{\exp(j\phi_c)P(d)}\right| \tag{11}$$

We deduce from (11) that minimizing the CFO error is equivalent to maximizing $f(d)$: = $|d \cdot P(d)|$. Keeping in mind that the large d increases a buffer size, we find the optimal delay, which is the smallest d satisfying $f'(d) = 0$. Then, the optimal d for the FSK PHY with the modulation index h: = $2f_dT$ can be approximated as

$$d^*_{\mathrm{CFO}} \approx \begin{cases} \frac{T}{4h-2} & h = 1 \\ \frac{T}{h}(1.5-h) & 0.5 < h < 1 \\ \frac{T}{h} & h \le 0.5 \end{cases} \tag{12}$$

On the other hand, there is a different optimal delay d for demodulation process. Considering that a bit decision of CDR performs at the center of $[nT + d,(n+1)T]$ in (5), the decision distance between bit 0 and 1 is calculated as $|\exp(j2\pi f_d d) - \exp(-j2\pi f_d d)| = 2\sin(2\pi f_d d)$ in the absence of CFO. Then, the optimal delay d is given by maximizing this distance as

$$d^*_{\mathrm{dem}} = \frac{1}{4f_d} = \frac{T}{2h} \tag{13}$$

It is observed from (12) and (13) that when h = 1, the optimal delay is $T/2$ for both cases, which enables reducing the digital logic by implementing the common path for CFO estimation and demodulation. Note that the mandatory FSK system of most WPAN standards uses h = 1.

When it comes to the case of $h < 1$, however, discordance between d^*_{cfo} and d^*_{dem} happens and it might introduce additional complexity due to different delay setting. Therefore, we suggest to set $d^*_{\mathrm{cfo}} = d^*_{\mathrm{dem}}$ even in the case of $h < 1$. To verify this, let us investigate $f(d)$ that determines the CFO error variance in (13) at $d = d^*_{\mathrm{dem}}$, given as

$$f(d^*_{\mathrm{dem}}) = \frac{T^2}{\pi h^2} \tag{14}$$

Since (14) is monotonically decreasing function according to the modulation index h, the CFO error

variance for $h < 1$ is always small enough compared with $h = 1$ case. Thus, $\eta(t; d^*_{\text{dem}})$for all $h \leq 1$can be used for our phase rotation vector estimation with negligible performance degradation.

3.3 Optimization on Delay *d*

We evaluate the probability of a bit error for our receiver based on (8), which is approximately calculated as

$$P_b \approx Q\left(\sqrt{\frac{\cos^2(\tilde{\phi}_c)\cdot E_b}{N_o}}\right) \tag{15}$$

where $\tilde{\phi}_c$ is a phase rotation due to a residual CFO and the noise variance is obtained from $\overline{w}(t)$. Note that $E_b \coloneqq 1$ and $N_o \coloneqq 2\sigma^2$ for our system model. Since the BER requirement for SUN system is 10^{-5} at SNR 15dB as discussed in Sec. II, the allowable CFO error for our FSK demodulator can be obtained by finding $\tilde{\phi}_c$ that satisfies the following

$$P_b\Big|_{\frac{E_b}{N_o}=15dB} \leq 10^{-5} \tag{16}$$

3.4 Summary

We summarize our three-stage FSK signal recovery process.

Step 1: Calculate the phase difference vector $c(t;d)$ with the optimal d.

Step 2: Calculate $\eta(t;d)$ to estimate the phase rotation vector by summation of $c(t;d)$.

Step 3: Compensate the phase rotation from $c(t;d)$, and then decide 0/1 by comparing the imaginary part with 0.

The major advantages of our scheme are the following.

1. Thanks to digital CFO compensation, the proposed receiver is affordable for recent FSK WPAN standards specifying the short preamble, such as SUN, LECIM and TVWS WPAN.
2. The common implementation path for CFO estimation and FSK demodulation enables to alleviate the complexity due to inevitable multi-bit ADC employment.
3. Unlimited CFO acquisition range is achieved by directly managing the CFO-induced phase distortion.

Ⅳ. Simulations

To verify the performance of the proposed FSK receiver, we conducted simulations. For comparison, we introduce the matched-filter based ideal FSK demodulator[8] and two existing schemes[6,7]. For all schemes, the bit rate is $1/T = 50$ KHz and $f_d = 25$ KHz with $h = 1$, as in IEEE 802.15.4g SUN standard[1]. For the receiver parameters, we considered $f_{\text{IF}} = 200$ KHz and $d = T/2$.

First, we determine the ADC bit resolution in Fig. 3, where the BER performance without CFO is illustrated. In addition to 1-bit CFC scheme[6], we modified the CFC to incorporate the multi-bit quantization for fair comparison. Since the decision distance for the proposed and CFC schemes is same in the absence of CFO, the corresponding BER performance is also same. It is observed from Fig. 3 that 1-bit scheme fail to meet the BER requirement. As a result, a multi-bit is essential for long-range WPAN applications and we suggest 3-bit ADC. We also examined the 2-bit and 3-bit quantized SPADC schemes[7], where both show relatively poor performance. Note that the proposed and CFC receivers used 400 KHz sampling rate while the SPADC receiver utilized 3.2 MHz and 12 MHz for 2-bit and 3-bit case for its proper operation.

Figure 4 compares the averaged CFO estimation error defined as $E[|f_o - \hat{f}_o|]$ at target SNR range. Since the 15.4g SUN standard specifies the maximum frequency tolerance of ±50 ppm[1], we considered the maximum 100 ppm at 915 MHz carrier frequency. Since the allowable CFO error can be found as 7 KHz based on (16) and its approximation loss, we suggest 1-byte ($M = 4$) preamble for CFO estimation. It is observed from Fig. 4 that the proposed scheme achieves negligible CFO estimation error regardless of the amounts of

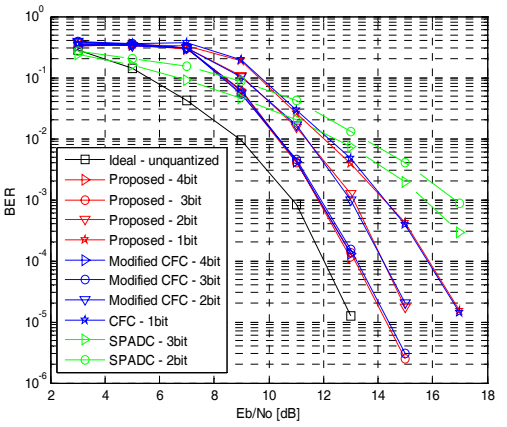

그림 3. CFO 영향이 없을 때 ADC 유효비트에 따른 BER 성능 비교
Fig. 3. BER performance according to ADC bit resolution in the absence of CFO

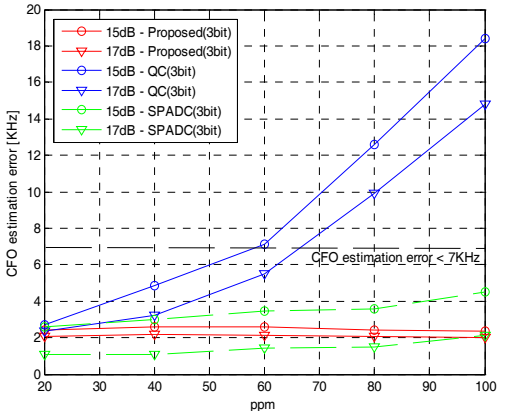

그림 4. 1-Byte Preamble을 사용했을 때 평균 CFO 추정 오차 비교
Fig. 4. Averaged CFO estimation error with 1-byte preamble

CFO, which confirms the advantage of full acquisition range on CFO estimation. We also investigated the performance of CFO estimator for the 3-bit SPADC scheme, where the error is small at high SNRs. In contrast, the CFO estimator[6] used the QC scheme, which requires its own digital logic in addition to CFC based demodulator, and it shows increased estimation error as CFO increases.

Figure 5 plots the BER performance at various CFOs, where the proposed scheme achieves CFO-free performance and satisfies the BER requirement. Since the CFO estimation error keeps intact regardless of CFO as shown in Fig. 4, our

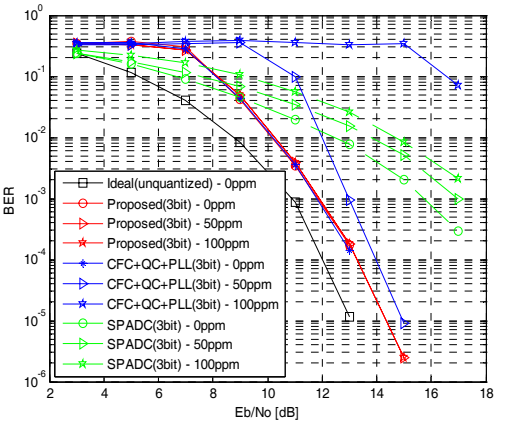

그림 5. CFO 영향이 있을 때 BER 성능 비교
Fig. 5. BER performance in the presence of CFO

FSK receiver achieves CFO-free BER performance. Although the 3-bit SPADC scheme also reveals nearly CFO-free performance, it is not suitable for recent WPAN applications since it fails to satisfy the BER 10^{-5} at SNR 15dB and requires relatively high sampling rate. On the other hand, the modified 3-bit CFC + QC + PLL scheme shows limited performance since the CFO estimation error for the QC-based CFO estimator dramatically increases for large CFO, as in Fig. 4. Notice that we modeled the ideal PLL by assuming no delay due to loop filter.

Ⅴ. Conclusion

We have proposed the digital FSK receiver for WPAN applications covering 1 Km. Relying on CFO correction with full acquisition range, the resulting scheme can satisfy the target BER with the short preamble at large CFO, which makes it attractive for recently emerging long-range WPAN applications.

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