論 文

Non-Persistent CSMA방식에 의한 지역망 Controller

正會員 金 商 雲* 正會員 金 韓 柱**

A Simple Local Area Network Controller by Non-Persistent CSMA

Sang Woon KIM* *and* Han Joo KIM**, *Regular Members*

요 약 Nonpersistent CSMA제어절차에 의하여 지역망 콘트롤러를 제작하였으며 버퍼 레지스터를 사용하여 마이크로 컴퓨터와 인터페이스시켰다. 네트워크 로우드의 변화에 대한 버스의 이용률을 최적화시키기 위하여 패킷 재송신 시간을 2^n의 함수로 조정하였다. 메시지는 패킷으로 만들어져 128바이트씩 버스에 전송되며 물리층에서 최대 데이타 전송 속도는 19,200bps를 얻었다.

ABSTRACT A local area network(LAN) controller is designed according to non-persistent CSMA protocols. By means of a buffer register, a microcomputer interfaces with the LAN controller. To keep bus utilization near the optimal efficiencies, the transmission intervals are adjusted as a function of 2^n. A message in the form of a packet consisting of 128 bytes is transitted to the bus. The maximum transmission rate of 19.2 Kbps is obtained at layer 1.

1. INTRODUCTION

Non-persistent carrier sense multiple Access (CSMA) is used in the network control.

This protocol, before transmission of data, senses the channel. If no one else is transmitting, the station opens up itself. However, if the channel is already in use, it waits a random period of time and then repeats the algorithm. This algorithm leads to better channel utilization, but it has longer delays than 1-persistent CSMA.[1] The controller is organized as a series of layers which are physical, data link, and network layers. The transport and application layers are to be implemented on the host computers. This model is based on the proposal developed by the ISO (international standards organization).[1,4] The physical layer is concerned with converting parellel to serial data, checking the status of network bus, receiving the traffic jam, and setting the collision detection flags. The functions of data link layer are sending/receiving the packets to/from the bus. When the collision occurred, the retransmissions are controlled by the nonpersistent CSMA protocols. The network layer determines the characteristics of the controller-host computer interface. What this layer of software does, basically, is to accept messages from host computer, and convert them to packets which are available between controllers.

The packet size consists of 128 bytes.

*,** 延世大學校 工科大學電子工學科
Dept. of Electronic Engineering, Yonsei University, Seoul, 120 Korea.
論文番號 : 84-20 (接受 1984. 2. 8)

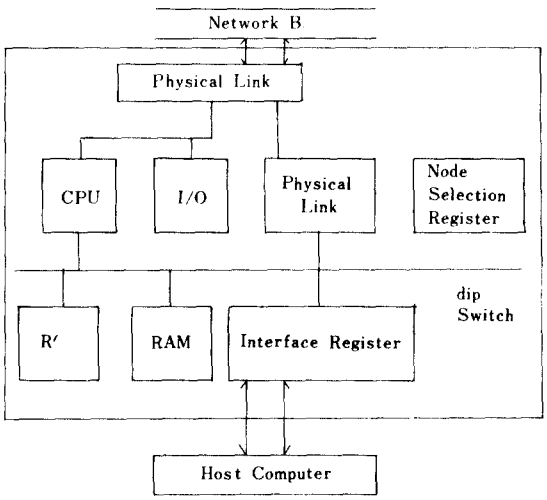

Fig. 1 Hardware structure of LAN controller (5).

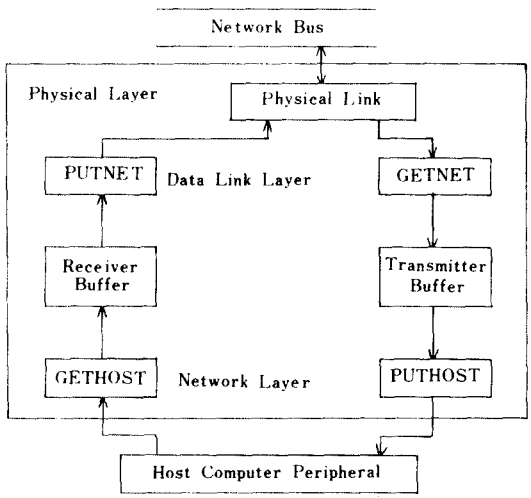

Fig. 2 Software structure of LAN controller (5).

2. LAN CONTROLLER

2.1 HARDWARE

The LAN Controller consists of CPU, ROM(2 KB), RAM(1KB), I/O, and TTL gates. Memory-mapped I/O is used and the system reserves a portion of the total address space for I/O ports.(2) The number of nodes is selected by dip switch. The hardware organization is shown in Figure 1.

Physical link layer consists of I/O (i8251) and TTL gates. The layer is accessed through a bus buffer. The physical link register uses bit 0 for checking the NET busy and transmitting the JAM. The time constants of JAM and NET busy are 2ms and 4ms respecitively. Bit 1 is the flag of collision detection(CD) which is carried out through comparing the transmission data and network bus data. Bit2 decides the waiting time for retransmission. The time constant of weight flag is 12 ms. The weight time for packet retransmission is the function of (2^n) for optimal utility of the bus.

By means of interface register, the LAN Controller interfaces with the microcomputer system. In the interface register, there are input and output registers.

In the data transfer from host computer to LAN Controller the input register uses two addresses for data and command. The low address is used for data and high address for command. The data transfer to the host computer is the same as LAN Controller. For the status register, it has full, data/command, and empty flags in the register.

2.2 SOFTWARE

The software structure is shown in Fig 2. Data link and network layer are implemented with software which consists of transmit and receive processes. The parallel processing of these processes uses RRJ (register relative jump) in the Z80 CPU. The RRJ has the return address of each process.

LAN Controller have transmit and receive buffers. The buffer can receive the three packets simultaneously.

The programs of Table 1 to 4 process the functions of GETHOST, PUTNET, PUTHOST and GETNET respectively.

3. EXPERIMENTS

In this paper, experiments are carried out by an OSM microcomputer system and an AmSYS 29/10 microcomputer system. The OSM microcomputer has a Z80 CPU and AmSYS 29/10 microcomputer has an i8080 CPU. The OS of the two systems is CP/M.

In the grobal multiple access bus, the network of two microcomputer systems needs the two LA-

Table 1 Transmission Flow of Network Layer.

```
Function (GETHOST)
11 : wait while buffer full;
     reset counter;
12 : wait until register full;
     if DATA then
        if conuter=0 then
           begin
        write DEST; write SOURCE;
        write TYPE; end;
        write DATA; counter increment;
        if counter less than 128 then go to 12;
        wait until register full;
        go to 13;
        else(CMD)
          if CMD more than equel 80H then
            begin write DONE; go to 12; end;
        else
          if OFFH more than CMD then
            begin AND 7FH; write TYPE; go to 12;
          end;
          else
            begin set END flag; go to 13; end;
13 : write LENGTH;
     set BUFFER FULL;
     buffer increment;
     go to 11;
```

N Controller which have the same structure except for interface register. The structure of interface register depends upon host computer. The LAN Controller is implemented on S-100 bus board in the OSM microcomputer system. The AmSYS 29/10 microcomputer system uses connector from which data address and control signals are derived.

The control program is developed with Z80 macro-assembler. Transmit command T, receive command R, and end command E are carried out through the keyboard.

The performance of LAN depends upon the transmission rate of data and the number of node. Although the LAN is not implemented with a large number of microcomputer systems, the two microcomputer systems proved the main functions of LAN Controller satisfactorily.

Table 2. Transmission Flow of Data Link Layer.

```
Function (PUTNET)
11 : interval counter=1;
     wait until buffer full;
12 : wait while NET busy;
     if NET busy then go to 12
     CD flag reset;
     transmit PREAMBLE, DEST, SOURCE,
     LENGTH;
     if CD flag=1 then
       begin interval counter x 2; go to 12; end;
     else
       begin
         transmit DATA, SUM, POSTAMBLE;
         if  CD flag=1 then go to 12; end;
         reset BUFFER FULL;
         buffer increment;
         go to 11;
       end;
```

Table 3. Receive Flow of Data Link Layer.

```
Function (GETNET)
while true do
  begin
    wait until NET busy;
    synchronize;
    if error then LAM
    else
      begin
        receive DEST;
        if DEST SOURCE then
          begin
            receive SOURCE, TYPE, LENGTH;
            receive DATA;
            receive SUM;
            if SUM error then JAM
            else
              begin set buffer full;
                buffer increment;
              end;
          end;
      wait while NET busy;
  end;
```

Table 4. Receive Flow of Network Layer.

```
Function (PUTHOST)
11 : wait until buffer full;
     output NODE;
     output TYPE;
     if END type then set END flag;
12 : output DATA;
     if END flag is set then
       begin
         output EOF;
         reset BUFFER FULL;
         buffer increment;
         go to 11;
       end;
     else
       begin
         buffer increment;
         wait until buffer full;
         go to 12;
       end;
```

The collision detection and time delay are not implemented in this study. The speed of data transmission is 19.2 kbps at layer 1 using the programmable I/O device.

4. CONCLUSION

In this paper, a bus network is designed with LAN Controllor which uses the global multiple access bus and shows that it is possible to transfer files, exchange messages and share resources between microcomputer systems.

The network interface program which runs on a CP/M is developed. The CP/M has not the function of network management and it needs the interface process between the nodes which exchange the messages.

It should be studied the function of network management systems in the CP/M. It may be accomplished with modifying BIOS. The data transmission rate may be increased by using VLSIchips or high performance chips.

REFERENCE

(1) A. S. Tannenbaum, "Computer networks," Prentice-Hall, Inc., pp. 286-306, 1981.

(2) C. Weitzman, "Distributed micro/minicomputer systems : structure, implementation and application," Prentice-Hall, Inc., pp. 21-97, 1980.

(3) M. M. Robert, et al, "Ethernet : Distributed packet switching for local computer networks," Comm. of ACM, vol. 19, no. 7, Jul. 1976.

(4) H. Zimmermann, "OSI reference model-the ISO model of architecture for open systems interconnection," Ibid, pp. 425-432, Apr., 1980.

(5) K. Mashaki, et al, "Design of local network controller," Interface, pp. 209-216, Aug., 1983.

金 商 雲(Sang Woon KIM) 正會員
1956年 3月13日生
1978年 : 韓國航空大學通信工學科卒業
1980年 : 延世大學校大學院電子工學科卒業
現在 : 延世大學校大學院電子工學科在學中

金 韓 柱(Han Joo KIM) 正會員
1959年 5月18日生
1982年 : 延世大學校電子工學科卒業
1984年 : 延世大學校大學院電子工學科卒業
現在 : 金星半導體株式會社研究員