

LDPC 부호 구조에 따른 비트 패턴드 미디어 기록장치 시스템의 성능

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Performance of Bit-Patterned Media Recording System According to LDPC Coding Structures

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요 약

차세대 자기 데이터 저장장치인 비트 패턴드 미디어 기록장치의 고밀도 성능을 달성하기 위해서는 아일랜드들 간의 간격이 줄어들어야 한다. 그러나 이러한 감소는 인접 심볼간 간섭 및 인접 트랙간 간섭의 영향을 증가시키며, 데이터 검출을 어렵게 만든다. 또한 데이터 저장장치 시스템은 다른 통신 시스템과는 달리 재전송이 불가능하기 때문에 데이터 저장장치의 디코딩 실패의 확률은 매우 낮아야 한다. 본 논문에서는 비트 패턴드 미디어 기록장치에서 세가지 LDPC 부호 방식에 대한 성능을 비교한다. 오류를 정정하고 데이터 저장장치의 성능을 향상시키기 위하여 반복적 디코딩을 사용한 LDPC 부호는 중요한 기술로 사용된다. 유사한 시스템 구조와 부호율의 사용을 통해 세가지 LDPC 부호 구조의 성능을 확인한다.

키워드 : 비트 패턴드 미디어 기록장치, 연결 부호, 반복 부호, 저밀도 패리티 체크 부호, 곱 부호

Key Words : Bit-patterned media recording, concatenated code, iterative decoding, low-density parity check code, product code

ABSTRACT

To satisfy the demand for high areal density in bit-patterned media recording (BPMR) technology, which is a futuristic magnetics data storage system, the space between islands is reduced. However, this reduction causes intersymbol interference and intertrack interference, resulting in the corruption of data detection. In addition, because data storage systems encounter difficulty in retransmitting data unlike other communication systems, such systems require a low probability of decoding failure. In this paper, we compare the bit error rate performance of three types of low-density parity check (LDPC) coding structures for BPMR systems. To correct errors and improve the performance of data storage systems, LDPC codes with iterative decoding are used as an important technique. Using similar system structures and overall code rates, the three types of LDPC coding structures are simulated to verify performance.

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I. Introduction

Since the hard disk drive (HDD) technology was invented in 1956, its recording density has been tremendously increased by the HDD industry^[1]. However, the magnetic grains in magnetic storage systems should not be too small to fulfill the requirements of thermal stability, media writability, and the superparamagnetic limit^[2]. To overcome these problems and increase the recording density beyond 1 terabit per square inch (Tb/in²), bit-patterned media recording (BPMR) has gained prominence as a promising magnetic storage system. BPMR offers some advantages such as the moderation of track-edge noise and transitions, removal of non-linear bit shifts, and simplification of tracking^[3]. To increase the recording density of BPMR systems, it is necessary to reduce the space between islands for both the down- and cross-track directions. However, the unavoidable issues of intersymbol interference (ISI) and intertrack interference (ITI), i.e., two-dimensional (2-D) ISI, degrade the system performance.

To resolve these problems, signal-processing techniques such as signal detections, error control codes, and modulation codes have been proposed by many researchers. To avoid the patterns that cause a 2-D ISI, modulation-coding schemes have been studied^[4]. To help detect the received data, the partial-response maximum-likelihood method is applied to data storage systems where the channel response is equalized to a partial-response pulse-shape and maximum-likelihood sequence detector^[5]. To obtain a substantial bit error rate (BER) performance, concatenated code schemes using a low-density parity check (LDPC) code, polar code, etc., have been proposed^[6]. In addition, because it is difficult for data storage systems to retransmit data unlike other communication systems, such systems require a low probability of decoding failure. To correct errors and improve the performance of data storage systems, LDPC codes with iterative decoding are used as an important technique. In this paper, we compare the BER performance of three types of LDPC coding

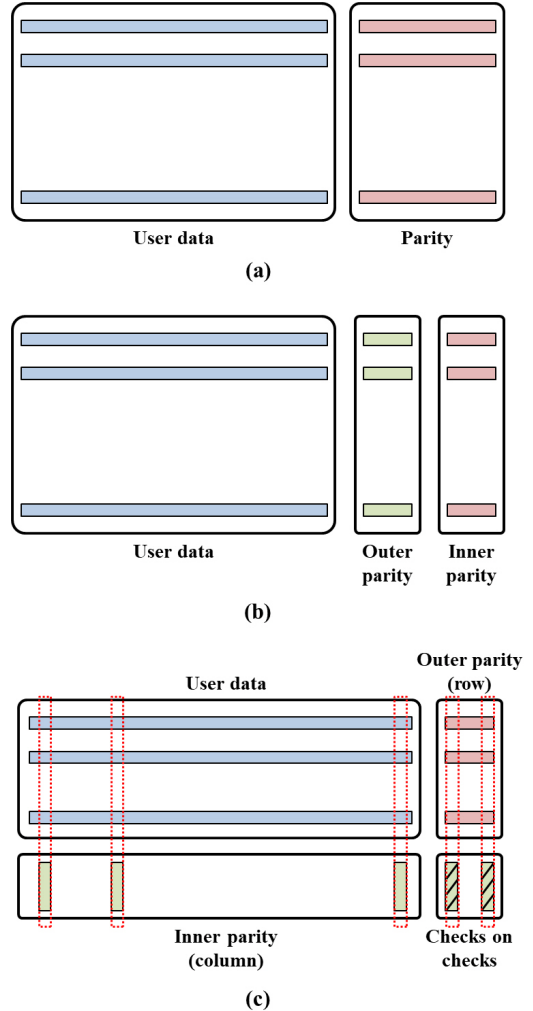


그림 1. 3가지 부호 방식 (a) LDPC 부호만 사용, (b) 연결 부호, (c) 곱 부호

Fig. 1. Three types of code structures. (a) LDPC code alone, (b) concatenated code, (c) product code.

structures for BPMR systems. Using similar system structures and overall code rates, the three types of LDPC coding structures, an LDPC code alone, as shown in Fig. 1(a), two concatenated LDPC codes, as shown in Fig. 1(b), and two-product LDPC codes, as shown in Fig. 1(c), are simulated to verify performance.

II. Three Types of LDPC Decoding Structures

To verify the BER performance according to the

LDPC coding structures, we compare the three structures. They are referred to as case (1), which is an LDPC code alone, case (2), which is two concatenated LDPC codes, and case (3) which is two-product LDPC codes. Fig. 2 shows the system block diagram, where i_{dec} is the predefined number of iterations between the inner and outer decoders. For case (1), as shown in Fig. 2(a), the extrinsic information generated at the LDPC decoder output is fed back to the LDPC decoder input in the next iteration after finishing an LDPC decoding procedure. In case (1), the LDPC (4096, 3616) code is used, and the overall code rate is 0.8828.

Case (2) is a concatenated coding scheme, which combines two LDPC codes with different code rates by serial connection, as shown in Fig. 2(b). In the concatenated code, the user data u is first encoded by the outer code $C1 (n_1, k)$ and then encoded by the inner code $C2 (n_1, n_2)$. The decoding procedure is performed in the reverse order. After the output

of the channel detector is decoded by the inner decoder, the extrinsic information generated by the inner LDPC decoder is fed to the outer LDPC decoder. Then, the output of the channel detector including the extrinsic information is decoded by the outer decoder. The extrinsic information generated by the outer LDPC decoder is fed to the inner LDPC decoder to assist it. When i_{dec} is equal to the maximum limit, this iteration process terminates and the outer decoder outputs the final decision value. In case (2), the LDPC (3856, 3616) code as the outer code and the LDPC (4096, 3856) code as the inner code, are used and the overall code rate is 0.8828.

Case (3) is a product coding structure, which was introduced by Elias in 1954^[7]. It combines two systematic LDPC codes with the same code rate, as shown in Fig. 2(c). In the product code structure^[6], the codeword of the outer code $C1 (n_1, k_1)$ is arranged into the rows of a rectangular array. Then, the codeword of the inner code $C2 (n_2, k_2)$ is arranged into the columns of the rectangular array. The decoding procedure is performed in the reverse order and is similar to the decoding procedure of the concatenated code. In case (3), two LDPC (4096, 3856) codes, as the outer and inner codes, respectively, are used and the overall code rate is 0.8862.

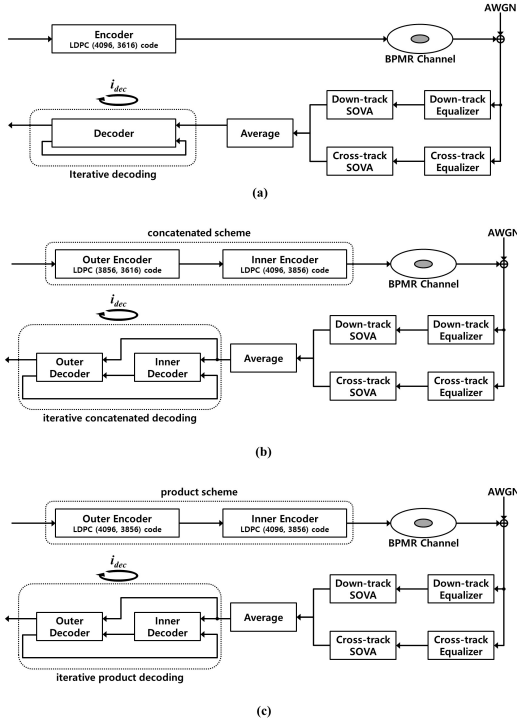


그림 2. 3가지 부호 방식에 대한 블록 다이어그램 (a) LDPC 부호만 사용, (b) 연결 부호, (c) 곱 부호
Fig. 2. Block diagram of three types of code structures. (a) LDPC code alone, (b) concatenated code, (c) product code.

III. BPMR Channel Modeling

We consider a discrete-time BPMR system for a read-channel model, which introduces the ITI and ISI. The channel coefficient $h_{m,n}$ is obtained by sampling the 2-D Gaussian island pulse response as follows^[8],

$$h_{m,n} = A \exp \left\{ -\frac{1}{2c^2} \left[\left(\frac{mT_z}{PW_z} \right)^2 + \left(\frac{nT_x}{PW_x} \right)^2 \right] \right\}, \quad (1)$$

where A represents the normalized peak amplitude; the constant c is $1/2.3548$, which is derived from the relationship between the standard deviation of a Gaussian function and $PW50$ which is a parameter of the pulse width at half the peak amplitude; T_x and

T_z are the bit period and track pitch, respectively; PW_z and PW_x are the PW50 of the cross- and down-track pulses, respectively. A readback signal $r_{p,q}$ of the BPMR system is given by,

$$r_{p,q} = d_{p,q} \otimes h_{m,n} + n_{p,q} = \sum_{m=-N}^N \sum_{n=-N}^N d_{p-m,q-n} \cdot h_{m,n} + n_{p,q}, \quad (2)$$

where the data $d_{p,q} \in \{-1, +1\}$ is encoded by encoders; the signal $r_{p,q}$ is the readback signal on the q th data bit along the p th track; \otimes is the 2-D convolution operator; $n_{p,q}$ is the electronic noise modeled as an additive white Gaussian noise with zero mean and variance σ^2 ; N is the length of the interference from neighboring islands.

IV. Simulation and Results

In this simulation, we compare the BER performance of the system according to the signal to noise ratio (SNR) values in case (1), case (2), and case (3). We have assumed that the data is read per page, where 2 pages have been simulated, and each page comprises 4096×4096 bits. The down-track direction island length L_x and cross-track direction island length L_z are 11 nm, each. To achieve an areal density of 2 Tb/in², we set the bit period T_x and track pitch T_x to 18 nm, each. PW_x and PW_z are set to 19.4 nm and 24.8 nm, respectively, to achieve the 2-D Gaussian island pulse response. Further, since the interference from the islands in $N = 2$ is almost negligible, we assume $N = 1$ for reducing the complexity of the system. To control the 2-D ISI and detect the signal, the soft output Viterbi algorithm is used^[5].

Fig. 3 presents the BER performance of case (1) in accordance with the number of iterations when i_{dec} assumes a value ranging from 0 to 3. As the number of iterations increases, the performance is enhanced. The performance of i_{dec} at the values of 2 and 3 is similar. Further, when i_{dec} is 3, the BER performance demonstrates the best results among the three cases. However, when the SNR is over 7.4 dB, an error floor is encountered. Fig. 4 illustrates the BER performance of case (2) depending on the

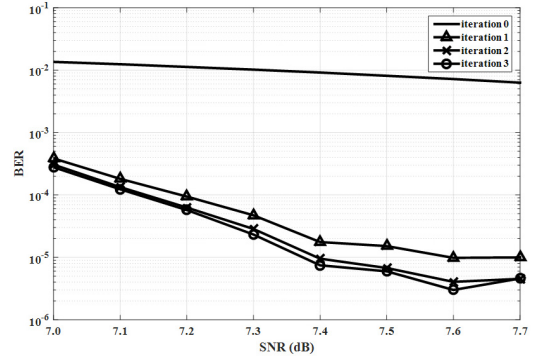


그림 3. Case (1)에서 반복 횟수에 따른 BER 성능
Fig. 3. The BER performance of case (1) in accordance with the number of iterations.

number of iterations when i_{dec} assumes a value ranging from 0 to 3. As the number of iterations increases, the performance also improves. The performance of i_{dec} at the values of 2 and 3 is similar. In case (2), the BER performance of i_{dec} at 3 demonstrates the best performance among the three cases. Fig. 5 shows the BER performance of case (3) according to the number of iterations. The performance exhibited when the number of iterations is 1 or higher is better than that exhibited when the number of iterations is 0. Further, when the SNR is over 7.5 dB, an error floor is encountered. However, when the SNR is over 9 dB, no errors occur. This demonstrates that the detection block must provide reasonable values to the LDPC decoding block to guarantee acceptable error rates.

In Fig. 6, we compare the BER performance of the three cases when i_{dec} is 3. Case (1) and case (3)

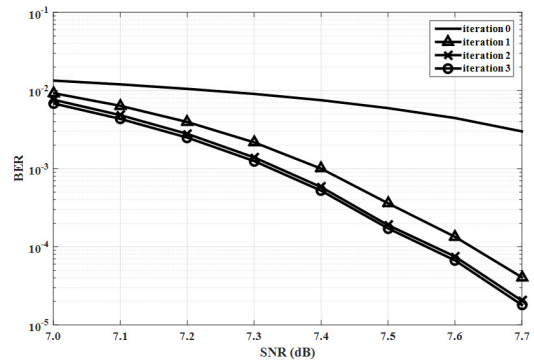


그림 4. Case (2)에서 반복 횟수에 따른 BER 성능
Fig. 4. The BER performance of case (2) in accordance with the number of iterations.

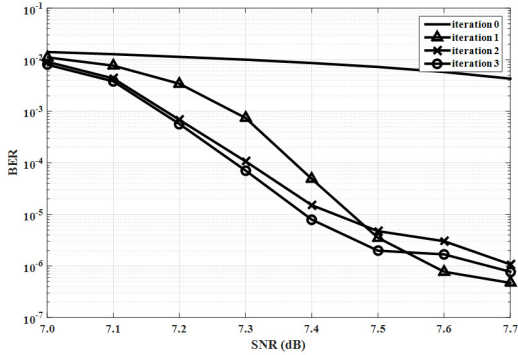


그림 5. Case (3)에서 반복 횟수에 따른 BER 성능
 Fig. 5. The BER performance of case (3) in accordance with the number of iterations.

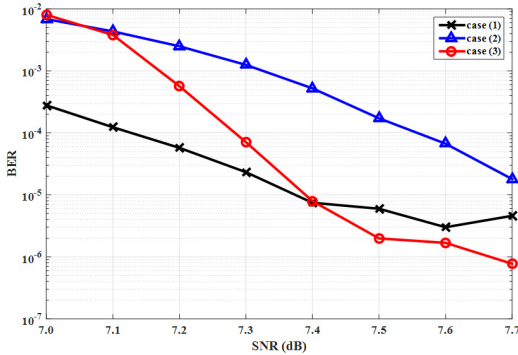


그림 6. i_{dec} 이 3일 때 3가지 구조의 BER 성능
 Fig. 6. The BER performance of the three cases when i_{dec} is 3.

achieve a better performance than that of case (2). While the BER performance in case (1) is better than that in case (3) in the low SNR region, the BER performance in case (3) is better than that in case (1) in the other SNR regions. However, the reason for a better BER performance in case (1) compared to that in case (3) in the low SNR region is considered to be an inaccuracy of the extrinsic information value in case (3), originating from the code rate. Therefore, if the product coding scheme is designed carefully, an improved error correcting capability can be obtained.

V. 결론

This paper compares the BER performance of three types of LDPC coding structures for BPMR systems using similar system structures and similar

overall code rates. The performance of the system changes depending on the decoding structure. The performance of the system using the product coding scheme is better than that using the LDPC code alone and the concatenated coding scheme. In addition, in case (1) and case (2), as the number of iterations increases, the performance of the system is enhanced due to the use of extrinsic information and iterative decoding between the LDPC decoders. However, in the high SNR region in case (3), we observed that the performance exhibited when the number of iterations is 2, is better than that exhibited at other values. The result indicates that it is not necessary to achieve many iterations. It also indicates that the extrinsic information generated during the iterative decoding process between the decoders should be utilized appropriately.

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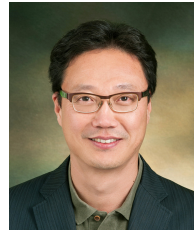


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