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엇갈린 형태의 비트 패턴드 미디어 기록장치를 위한 반복적 연접 부호 방식

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Iterative Concatenated Coding Scheme for Staggered Bit-Patterned Media Recording

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요 약

비트 패턴드 미디어 기록장치는 리소그래피 방식에 따라 일반적인 형태 혹은 엇갈린 형태로 하나의 비트를 저장하는 아일랜드의 배열이 가능하다. 일반적인 형태와 엇갈린 형태의 가장 큰 차이점은 인접 트랙간 간섭의 영향인데, 일반적인 형태에서는 메인 트랙의 아일랜드는 바로 위의 트랙과 아래 트랙의 아일랜드와 인접하게 된다. 하지만 엇갈린 형태에서는 메인 트랙의 아일랜드는 위의 트랙과 아래 트랙의 아일랜드보다 비트간 간격에서 반주기 정도 이동되어 있기 때문에 인접 심볼간 간섭이 줄어든다. 본 논문에서는, 엇갈린 형태의 비트 패턴드 미디어 기록장치를 위한 반복적 연접 부호 방식을 제안한다. 제안하는 연접부호 방식은 inner 부호와 outer 부호로 구성되어 있으며 두 부호간의 부가 정보를 반복적으로 사용하여 비트 패턴드 미디어 기록장치의 성능을 높일 수 있다.

키워드 : 비트 패턴드 미디어 기록장치, 연접 부호, 반복적 디코딩, 저밀도 패리티 체크 부호, 연판정 출력 비터비 알고리즘

Key Words : Bit-patterned media recording, concatenated code, iterative decoding, low-density parity check code, soft output Viterbi algorithm.

ABSTRACT

The layout of bit islands in bit-patterned media recording (BPMR) can be arranged in various structures such as regular- and staggered-array bit patterns according to the lithography approach. The main difference between the regular- and staggered-array bit patterns is the effect of inter-track interference. In this paper, we propose an iterative concatenated coding scheme using the three-path soft output Viterbi algorithm for a staggered BPMR system. The proposed concatenated coding scheme, which consists of inner and outer low-density parity check (LDPC) codes, can help improve the performance of BPMR because of the iteration between the inner and outer codes using extrinsic information.

Ⅰ. Introduction

To satisfy the requirement of storing tremendous amounts of data, the areal density (AD) of a hard disk drive (HDD) has been dramatically increased by the HDD industry[1]. However, because

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conventional HDDs that use perpendicular magnetic recording suffer from the problems of thermal stability, superparamagnetic limit, and so on, the bit-patterned media recording (BPMR) system is a promising candidate for the next generation of data-storage system to achieve AD beyond one terabit per square inch (Tb/in^2)[2]. Each island stores one bit that is recorded on the bit-patterned media (BPM) in a BPMR, whereas ensemble of grains stores one bit that is recorded on granular media. Thus, in contrast to the granular media, BPM offers the advantages of increased thermal stability and reduced nonlinear transition shift and transition noise[3]. To resolve these problems in terms of signal processing, many researchers have proposed signal detection, modulation-code schemes, and error-correcting codes (ECCs)[4,5].

However, the abovementioned schemes are only considered in a regular-array BPM layout. In a BPMR system, a BPM layout can be arranged on a regular array (regular-array islands), as shown in Fig. 1(a), or a staggered array (staggered-array islands), as shown in Fig. 1(b), according to the lithography approach (patterning process)[6]. The major difference between the regular- and staggered-array BPM layouts is the ITI effect. In a regular-array BPM layout, two islands affect the island on the main track, i.e., the island along the upper track and that along the lower track, which are located immediately from the island on the main track. However, in a staggered-array BPM layout, four islands affect the island on the main track, i.e., two islands along the upper track and two islands along the lower track, which is shifted from the island on the main track. Therefore, because the staggered-array BPM layout can reduce the ITI effect compared with the regular-array BPM layout, the performance using the staggered-array BPM layout is better than that using the regular-array BPM layout. Hence, suitable signal processing techniques for the staggered-array BPM layout are needed to enhance the staggered BPMR performance.

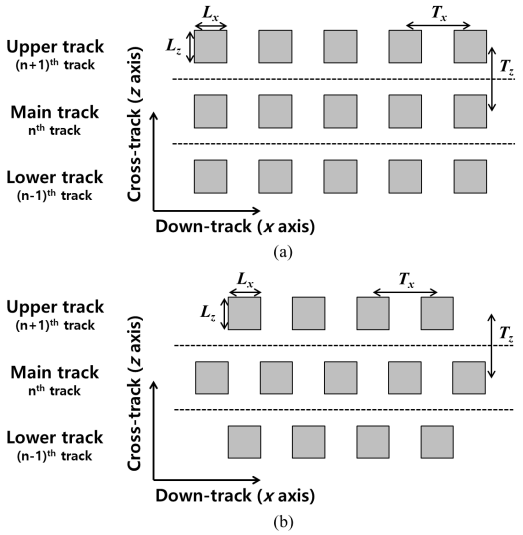

그림 1. 리소그래피 방식에 따른 BPM 레이아웃 (a) 일반적인 형태, (b)엇갈린 형태
Fig. 1. Configuration of (a) regular-array BPM layout and (b) staggered- array BPM layout according to the adopted lithography approach.

Ⅱ. Three-Path Sova Detection and Proposed Concatenated LDPC Coding Scheme

2.1 Three-Path SOVA Detection

To consider the ITI effect in staggered BPMR, the 3P SOVA scheme, which consists of three SOVAs, is proposed for signal detection of the staggered BPMR. Fig. 2 shows the block diagram of the proposed system. After the received data $r_{p,q}$ from the qth data bit along the pth track is equalized by an equalizer in down-track direction x, output $e_{p,q}$ is decoded by the SOVA in down-track direction x. In a similar manner, the output $e'_{p,q}$, which is equalized by an equalizer in cross-track direction z,

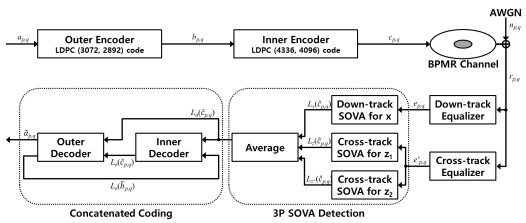

그림 2. 3P-SOVA를 사용한 제안하는 연접 LDPC 부호 방식의 블록 다이어그램
Fig. 2. Block diagram of the proposed concatenated LDPC coding using 3P SOVA.

is decoded by the SOVA in cross-track directions z_1 and z_2. Each SOVA in the x, z_1, and z_2 directions, as shown in Fig. 3, calculate branch metric $\lambda_{p,q}$ as follows[7]:

$$\lambda_{p,q}(s_j,s_k)=\{e_{p,q}-(f_{2,1}\cdot t_{p,q-1}(s_j)+f_{2,2}\cdot t_{p,q}(s_j)+f_{2,3}\cdot t_{p,q+1}(s_k))\}^2, \quad (1)$$

$$\lambda_{p,q}(s_j,s_k)=\{e'_{p,q}-(f_{1,2}\cdot t_{p-1,q}(s_j)+f_{2,2}\cdot t_{p,q}(s_j)+f_{3,2}\cdot t_{p+1,q}(s_k))\}^2, \quad (2)$$

$$\lambda_{p,q}(s_j,s_k)=\{e'_{p,q}-(f_{1,2}\cdot t_{p-1,q+1}(s_j)+f_{2,2}\cdot t_{p,q}(s_j)+f_{3,2}\cdot t_{p+1,q+1}(s_k))\}^2, \quad (3)$$

where f, s_j, s_k, $t(s_j)$, and $t(s_k)$ are the PR target coefficient, current state, next state, decisions at s_j, and decisions at s_k, respectively. After the 3P SOVA separately processes the three 1D SOVAs in the down-track direction and two cross-track directions z_1 and z_2, log-likelihood ratio (LLR) $L_a(\hat{c}_{p,q})$ is averaged by

$$L_a(\hat{c}_{p,q})=(L_x(\hat{c}_{p,q})+L_z(\hat{c}_{p,q})+L_{z'}(\hat{c}_{p,q}))/3 \quad (4)$$

where $L_x(\hat{c}_{p,q})$, $L_z(\hat{c}_{p,q})$, and $L_{z'}(\hat{c}_{p,q})$ are the LLR values decoded by each SOVA in the x, z_1, and z_2 directions, respectively.

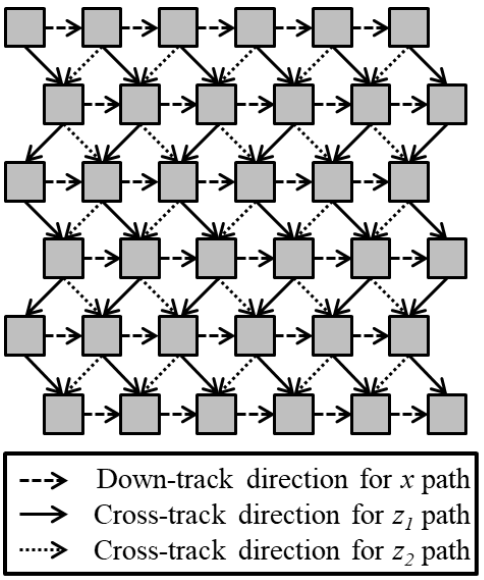

그림 3. x, z_1, z_2 방향에 따른 3P-SOVA의 구조
Fig. 3. Configuration of the 3P SOVA in the x, z_1, and z_2 directions [7].

2.2 Concatenated LDPC coding

Fig. 4 shows the encoding structure of the proposed concatenated LDPC coding scheme. The characteristic of the staggered-array BPM layout is considered by the proposed scheme. User data $a_{p,q}$ are encoded by the outer and inner LDPC encoders. After readback signal $r_{p,q}$ is processed by the 2D equalizers and 3P SOVA, the proposed decoding process (as shown in Fig. 2) begins as follows. (1) LLR value $L_a(\hat{c}_{p,q})$ from the 3P SOVA and extrinsic information $L_e(\hat{b}_{p,q})$ are decoded by the inner LDPC decoder. (In the first iteration between the inner and outer decoders, extrinsic information $L_e(\hat{b}_{p,q})$ is zero.) (2) The outer LDPC decoder is implemented using extrinsic information $L_e(\hat{c}_{p,q})$ from the inner LDPC decoder and LLR value $L_a(\hat{c}_{p,q})$ from the 3P SOVA. (3) Then, Steps (1) and (2) are iterated, and the outer LDPC decoder outputs estimated data $\hat{a}_{p,q}$ using $L_a(\hat{c}_{p,q})$ and $L_e(\hat{c}_{p,q})$.

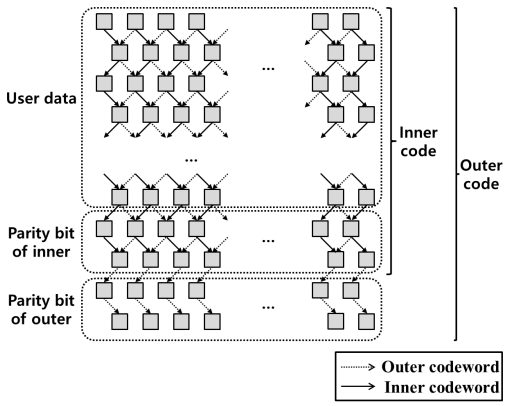

그림 4. 제안하는 연접 LDPC 부호의 인코딩 방식
Fig. 4. Encoding structure of the proposed concatenated LDPC coding scheme.

Ⅲ. Staggered BPMR Channel Modeling

We consider a read-channel model of the discrete-time staggered BPMR. Binary sequence $c_{p,q} \in \{-1, +1\}$ is passed through the staggered BPMR channel, which introduces ITI and ISI. Readback signal $r_{p,q}$ is further corrupted by electronics noise $n_{p,q}$, which is modeled as an additive white Gaussian

noise with zero mean and variance σ^2. Readback signal $r_{p,q}$ of the staggered BPMR is given by

$$\begin{aligned} r_{p,q} = & \sum_{n=-N}^{N} c_{p,\,q+n} \cdot h(0,n) \\ & + \sum_{m=0}^{\lfloor (N-1)/2 \rfloor} \sum_{n=-N+m+1}^{N-m} c_{p-(2m+1),\,q+n} \cdot h(-(2m+1), n-\frac{1}{2}) \\ & + \sum_{m=0}^{\lfloor (N-1)/2 \rfloor} \sum_{n=-N+m+1}^{N-m} c_{p+(2m+1),\,q+n} \cdot h((2m+1), n-\frac{1}{2}) \\ & + \sum_{m=1}^{\lfloor N/2 \rfloor} \sum_{n=-N+m}^{N-m} c_{p-2m,\,q+n} \cdot h(-2m,n) \\ & + \sum_{m=1}^{\lfloor N/2 \rfloor} \sum_{n=-N+m}^{N-m} c_{p+2m,\,q+n} \cdot h(2m,n) + n_{p,\,q}, \end{aligned} \tag{5}$$

where N is the length of the interference from the neighboring islands in the staggered-array BPM layout[8], m and n represent the indexes in the down- and cross-track directions, and $h(n, m)$ is the BPMR 2D channel island pulse response. In this study, because ISI and ITI effects from the islands are relatively negligible (almost zero) for $N \geq 2$, we set N = 1 to reduce complexity. BPMR 2D channel island pulse response $h(n, m)$, which is obtained by sampling the 2D Gaussian island pulse response, can be expressed as

$$h(m,\ n) = P(mT_z + \Delta_{off}, nT_x), \tag{6}$$

where $P(z, x)$ is the 2D Gaussian island pulse response; T_x and T_z are the bit period and track pitch, respectively; and Δ_{off} is the read-head offset. The TMR is calculated using the relationship between the head offsets and track pitch as follows[9]:

$$\text{TMR}(\%) = \frac{\Delta_{off}}{T_z} \times 100. \tag{7}$$

The 2D Gaussian island pulse response, i.e., $P(x, z)$, is expressed as[10]

$$P(x,z) = A \exp\left\{ -\frac{1}{2c^2} \left[\left(\frac{x}{\text{PW}_x} \right)^2 + \left(\frac{z}{\text{PW}_z} \right)^2 \right] \right\}, \tag{8}$$

where c is 1/2.3548, which represents the relationship between the standard deviation of a Gaussian function and PW50 (a parameter of the pulse width at half of the peak amplitude), and PW_x and PW_z are the PW50 of the down- and cross-track pulses, respectively.

Ⅳ. Simulation and Results

To evaluate the performance of the proposed concatenated LDPC coding, we used the staggered BPMR system at 2 Tb/in2. Island length L_x in the down-track direction and island length L_z in the cross-track direction were both 11 nm. Bit period T_x and track pitch T_x were both 18 nm. We set PW_x to 19.4 nm and PW_z to 24.8 nm for the 2D island pulse response. The signal-to-noise ratio (SNR) was defined as $10\log10(1/\sigma^2)$. We used the 2D 3 × 3 PR target as follows:

$$F = \begin{bmatrix} 0 & 0.15 & 0 \\ 0.20 & 1 & 0.20 \\ 0 & 0.15 & 0 \end{bmatrix}. \tag{9}$$

We used the 5 × 5 2D equalizer, and the equalizer coefficients were updated using the least mean square algorithm. We compared the performance of the proposed concatenated LDPC code using 3P SOVA, proposed concatenated LDPC code using 2D SOVA, and one LDPC (conventional LDPC) code using 3P SOVA. The size of the inner LDPC code was (4336, 4096), and that of the outer LDPC code was (3072, 2892). The size of one LDPC code was (4336, 3856). The number of iterations in the LDPC decoder was 10. The decoding algorithm used for the LDPC decoder was the standard sum‐product algorithm in the log domain.

Fig. 5 shows the BER performance of the concatenated LDPC coding scheme according to the SNR. The proposed concatenated LDPC that used the 3P SOVA exhibited performance gains of ~0.5 and ~1.4 dB over the concatenated LDPC that used the 2D SOVA and one LDPC that used the 3P SOVA, respectively, at a BER of 10^{-6}.

Fig. 6 shows the BER performance of the concatenated LDPC coding scheme in terms of the

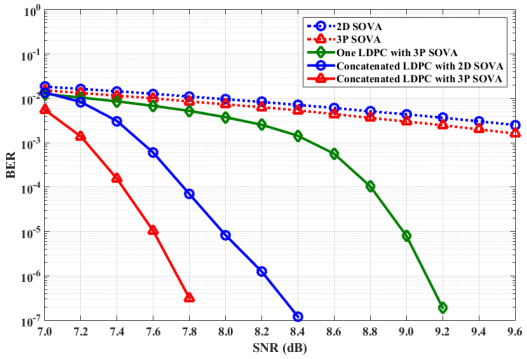

그림 5. SNR에 따른 제안하는 연접 부호의 BER 성능
Fig. 5. BER performance of the concatenated LDPC coding scheme according to the SNR.

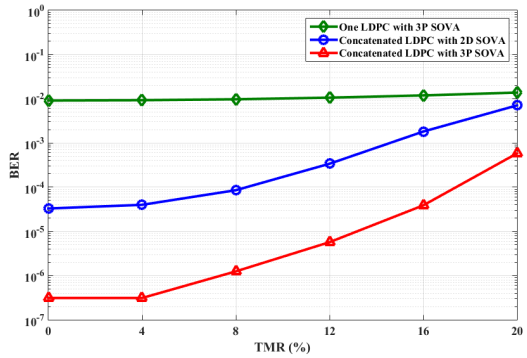

그림 6. TMR에 따른 제안하는 연접 부호의 BER 성능 (SNR = 7.8 dB)
Fig. 6. BER performance of the concatenated LDPC coding scheme according to the TMR (SNR = 7.8 dB).

TMR when SNR = 7.8 dB. The concatenated LDPC coding scheme that used the 3P SOVA showed better performance than the concatenated LDPC that used 2D SOVA and one LDPC that used the 3P SOVA.

V. 결 론

In this paper, we have proposed a multi-path concatenated LDPC coding scheme using the 3P SOVA for staggered BPMR. Because the islands in the neighboring tracks are displaced by a half-period from those along the main track in the staggered BPMR, in terms of ITI, the islands in the main track are mainly affected by the closest two islands in the upper track and two islands in the lower track. Therefore, the signal detection scheme and ECC for the staggered-array BPM layout are considered. From the simulation results, we demonstrated that the proposed multi-path concatenated LDPC coding scheme combined with the 3P SOVA and used with extrinsic information is suitable for the staggered BPMR system.

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