논문 19-45-02-01 The Journal of Korean Institute of Communications and Information Sciences '20-02 Vol.45 No.02
https://doi.org/10.7840/kics.2020.45.2.239

비트 패턴드 미디어 기록장치용 LLR 컨트롤러를 활용한 반복적 LDPC-SPC 곱부호

정 성 권◆, 이 재 진°

Iterative LDPC-SPC Product Code with LLR Controller for Bit-Patterned Media Recording

Seongkwon Jeong◆, Jaejin Lee°

요 약

비트 패턴드 미디어 기록장치는 제곱 인치당 1 테라비트 이상을 달성할 수 있기 때문에 차세대 저장장치로 주목받고 있다. 그러나 기록밀도의 증가를 위해서는 아일랜드들간의 간격이 감소되어져야 하는데, 이는 인접 심볼간 간섭과 인접 트랙간 간섭을 증가시킨다. 본 논문에서는 성능을 향상 시키기 위해 비트 패턴드 미디어 기록장치용 LLR 컨트롤러를 활용한 반복적 LDPC-SPC 곱부호 방식을 제안한다. 제안하는 곱 부호의 내 부호는 오류 정정 능력을 향상시키기 위해 LDPC를 사용하였으며, 외 부호는 코드율을 높이고 조정하기 쉽게 하기 위하여 SPC를 사용하였다. 또한 신드롬의 성질을 활용한 LLR 컨트롤러를 함께 사용하여 성능을 더욱 향상시켰다.

키워드 : 비트 패턴드 미디어 기록장치, 로그 우도비, 저밀도 패리티 체크 부호, 곱 부호, 단일 패리티 체크 부호

Key Words : Bit-patterned media recording, log-likelihood ratio, low-density parity check code, product code, single parity check code.

ABSTRACT

A bit-patterned media recording (BPMR) that can achieve an areal density of 1 terabit per square inch or higher is a type of future magnetic storage system. However, because the space between islands in both the down- and cross-track directions is reduced to extend the areal density, the effect of two-dimensional interference, which consists of both intersymbol and intertrack interference, is increased. This paper proposes an iterative low-density parity check (LDPC) - single parity check (SPC) product code with a log-likelihood ratio (LLR) controller for BPMR for bit-patterned media recording to improve the performance. The inner code improves the error correction ability by applying a LDPC code and the outer code increases the coding rate and flexibility by using a SPC code. The system performance is further improved by using an iterative algorithm between the inner and outer codes with LLR controller. The LLR controller, which uses the relationship between the syndrome and parity check matrix, receives the output of the LDPC decoder as input and modifies the LLR value to improve the performance. Simulation results indicate that the proposed product coding scheme with an LLR controller outperforms the existing product coding scheme without such a controller.

※ 이 성과는 정부(과학기술정보통신부)의 재원으로 한국연구재단의 지원을 받아 수행된 연구임(No. NRF-2019R1F1A1046899).
◆ First Author : Soongsil University, Department of ICMC Convergence Technology, seongkwon@ssu.ac.kr, 학생회원
° Corresponding Author : Soongsil University, Department of ICMC Convergence Technology, zlee@ssu.ac.kr, 종신회원
논문번호 : 201911-302-A-RN, Received November 18, 2019; Revised November 20, 2019; Accepted November 20, 2019

Ⅰ. Introduction

To satisfy the need for storing tremendous amounts of data, the areal density (AD) of a hard disk drive (HDD) has been drastically increased by the HDD industry[1]. However, because conventional HDDs using a perpendicular magnetic recording have inherent problems such as thermal stability and a superparamagnetic limit, the bit-patterned media recording (BPMR) system has become an alternative to the next generation of magnetic recording systems to extend the AD beyond one terabit per square inch (Tb/in^2)[2]. Each island stores one bit recorded on the bit-patterned media (BPM) through a BPMR, while an ensemble of grains stores one bit recorded on granular media. Thus, in contrast with granular media, BPM offers an improved thermal stability, a reduced transition noise, and a nonlinear transition shift[3].

Although a BPMR can overcome existing problems and offer the above advantages, it still faces certain challenges such as media noise, inter-symbol interference (ISI), inter-track interference (ITI), and track misregistration (TMR). Media noise, which includes island-size fluctuation and island-position jitter, is mainly caused by imperfections in the fabrication[2]. To increase the AD of a BPMR, the distance between islands in both the down- and cross-track directions must be reduced. Consequently, data detection is interrupted by two-dimensional (2D) ISI, which consists of ISI and ITI[4]. ISI and ITI eventually degrade the BPMR performance. The recording heads generally do not stay along the main track but close to it, resulting in a TMR. To resolve this problem in terms of signal processing, many researchers have proposed signal detection, modulation coding schemes, and error correcting codes (ECCs). To obtain an enhanced bit-error ratio (BER) performance, concatenated code schemes using a low-density parity check (LDPC) code or a polar code, among other code types, have been proposed[6],[8]. The proposed concatenated coding schemes exhibit a better BER performance than schemes using the LDPC code alone. To mitigate the ISI and ITI

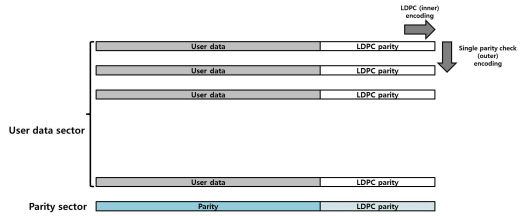

그림 1. 제안하는 LDPC-SPC 곱 부호의 구조
Fig. 1. The structure of the proposed product code structure with an inner code LDPC code and an outer SPC code.

present in the BPMR, 2D modulation coding schemes that can reduce an error pattern have been proposed[7,8].

In this paper, we propose an iterative product decoding scheme with a log-likelihood ratio (LLR) controller to improve the system performance. The structure of the product coding scheme consists of both an inner LDPC code and an outer single parity check (SPC) code, as shown in Fig. 1. An LLR controller that modifies the LDPC decoder output by using the relationship between the syndrome and parity check matrix is added. An iterative product decoding scheme with an LLR controller provides a better BER performance than an iterative product decoding scheme without an LLR controller or LDPC codes alone.

Ⅱ. Bpmr Channel Model

We consider a read-channel model of a discrete-time BPMR. Fig. 2 shows a block diagram of the proposed system model. After the binary data $t_{p,q} \in \{0, 1\}$ are converted into $d_{p,q} \in \{-1, +1\}$, $d_{p,q}$ is passed through the BPMR channel, which introduces ITI and ISI. A 2D Gaussian island pulse response $P(x, z)$, occurs, which is expressed as

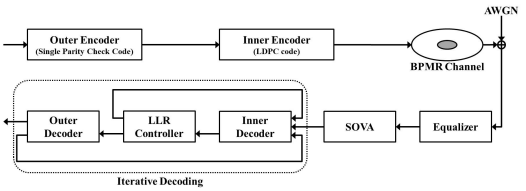

그림 2. 제안하는 시스템 모델의 블록 다이어그램
Fig. 2. Block diagram of the proposed system model.

follows[9]:

$$P(z,x) = A\exp\left\{-\frac{1}{2c^2}\left[\left(\frac{z}{\mathrm{PW}_z}\right)^2+\left(\frac{x}{\mathrm{PW}_x}\right)^2\right]\right\}, \quad (1)$$

where A is the normalized peak amplitude; the constant c, representing the relationship between the standard deviation of a Gaussian function and PW50, which is a parameter of the pulse width at half of the peak amplitude, is 1/2.3548; and PW_z and PW_x are the PW50 of the cross- and down-track pulses, respectively. We set PW_x to 19.4 nm and PW_z to 24.8 nm for the 2D island pulse response. The BPMR 2-D channel island pulse response $h(n, m)$, which is obtained by sampling the 2D Gaussian island pulse response, can be expressed as follows:

$$h(m,\ n) = P(mT_z,\ nT_x), \quad (2)$$

where $P(z,\ x)$ is the 2D Gaussian island pulse response, and T_x and T_z are the bit period and track pitch, respectively. A readback signal $r_{p,q}$ is further corrupted by electronic noise $n_{p,q}$, which is modeled as an additive white Gaussian noise (AWGN) with zero mean and variance σ^2. The readback signal $r_{p,q}$ of the BPMR is given by

$$\begin{aligned} r_{p,q} &= d_{p,q} \otimes h(m,n) + n_{p,q} \\ &= \sum_{m=-N}^{N}\sum_{n=-N}^{N} c_{p-m,q-n}\cdot h(m,n) + n_{p,q}, \end{aligned} \quad (3)$$

where the signal $r_{p,q}$ is the readback signal on the q-th data bit along the p-th track, $\otimes$ is the 2D convolution operator, $n_{p,q}$ is electronic noise modeled as an additive white Gaussian noise with zero mean and variance σ^2,and$N$ is the length of the interference from the neighboring islands. In this study, because the interference from the islands in N = 2 is mostly negligible, we assume N = 1 for simplicity.

Ⅲ. Proposed Iterative Product Decoding Scheme with LLR Controller

3.1 LLR CONTROLLER

Because LDPC decoding often fails in a low signal-to-noise ratio (SNR) region, the stopping criteria for the LDPC codes were proposed to predict a decoding failure and decrease the decoding complexity in a retransmission system, such as an automatic repeat request[10]. In the decoding of a linear block code, Syndrome **S**, which is a multiplication of codeword **c** and parity check matrix **H** (**cH**$^{\mathrm{T}}$**=S**), indicates not only whether a codeword is valid, but also the number of parity check constraints (i.e., the weight of the syndrome). In the decoding of the LDPC codes, the iterative decoding algorithm repeats until **cH**$^{\mathrm{T}}$**=0** or the maximum number of iterations has been reached. The proposed stopping criterion using the syndrome property helps reduce the number of iterations of the iterative decoding. In this study, we propose an iterative product decoding scheme using an LLR controller utilizing the syndrome property. After the LLR output of the LDPC decoder $L(\mathbf{C}_1)$ is changed to a hard decision vector **a**, **S** is computed as follows:

$$\mathbf{S} = \mathbf{a}\mathbf{H}^{\mathrm{T}}. \quad (4)$$

To modify the LLR value, coefficient β_i of the i-th position is calculated as follows:

$$\beta_i = \mathrm{d}_{\mathrm{H}}(\mathbf{h}_i, \mathbf{S}) / w(\mathbf{S}), \quad (5)$$

where $\mathrm{d}_{\mathrm{H}}(\mathbf{h}_i,\ \mathbf{S})$ is the Hamming distance between the i-th column $\mathbf{h}_i$ of **H** and **S**, and w(**S**) is the weight of the syndrome (or the number of 1s in **S**). Finally, the LLR output of the LDPC decoder $L(\mathbf{C}_1)$ at the i-th location is multiplied by β_i. However, because **S** = **0** (zero vector), indicating that a hard decision vector **a** has no error, we set β_i = 2. In addition, because **S** is the column of H corresponding to the location where a one-bit error in the codeword occurs, the one-bit error is

corrected, and we thus set β = 2.

3.2 Iterative Decoding with LLR Controller

Fig. 3 shows a flow chart of the proposed decoding scheme. After the iterative decoding between the LDPC decoder and the LLR controller is repeated three times, if the output of the LLR controller fails in the decoding, the failed sector samples from the third iteration output of the LLR controller are buffered for later iterative decoding. If the decoding of any sector is successful, its output of the LLR controller is used for calculating the following SPC constraint equation:

$$\sum_{all}^{i} a_{i,j} = \sum_{decoding\ failure}^{i} a_{i,j} + \underbrace{\sum_{decoding\ success}^{i} a_{i,j}}_{u_j} = 0, \tag{6}$$

$$\sum_{decoding\ failure}^{i} a_{i,j} = \sum_{decoding\ success}^{i} a_{i,j} = u_j, \tag{7}$$

where u_j is the partial syndrome accumulated from the data from a successful decoding. During the outer decoding procedure, the min-sum algorithm is applied to the failed sectors to update the LLR value as follows[11]:

$$\left|L_{k,j}(\mathbf{C}_2)\right| = \min_{failed\ sector\ excluding\ k}^{j} \left(\left|L^{*}_{k,j}(\mathbf{C}_1)\right|\right), \tag{8}$$

$$\mathrm{sgn}(L_{k,j}(\mathbf{C}_2)) = (2s_j - 1) \prod_{failed\ sector\ excluding\ k}^{j} \mathrm{sgn}(L^{*}_{k,j}(\mathbf{C}_1)), \tag{9}$$

where $L^{*}_{k,j}(\mathbf{C}_1)$ is the LLR value output from the output of the LLR controller at the third iteration. In addition, $L_{k,j}(\mathbf{C}_2)$, calculated using the min-sum algorithm, is applied to the LDPC decoder as a priori information. The iterative decoding among the inner LDPC decoder, the LLR controller, and the outer SPC decoder is repeated ten times. The proposed iterative product coding scheme for bit-patterned media recording helps improve the BER performance.

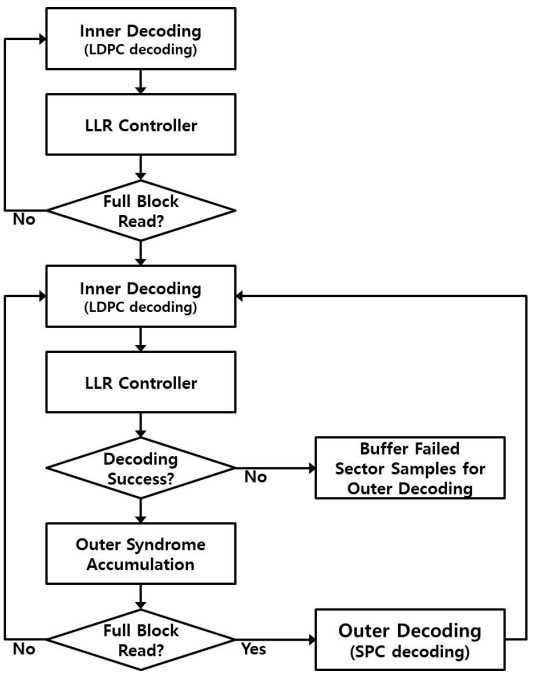

그림 3. 제안하는 디코딩 방식의 순서도
Fig. 3. Flow chart of the proposed decoding scheme.

Ⅳ. Simulation and Results

We assumed that the data are read per page, and that 100 pages are simulated. Each page has 4096 × 100 bits, and island lengths in the down-track direction L_x and cross-track direction L_z are both 11 nm. The bit period T_x and track pitch T_z are both 18 nm at 2 Tb/in^2.The SNR is generally measured in decibels (dB), and thus the SNR was defined as $10\log_{10}(A/\sigma^2)$ dB, where A = 1 is the peak value of the readback signal. We set an equalizer size of 5 × 5. The equalizer coefficients are updated using the least mean squares algorithm, and the soft output Viterbi algorithm is used for detection. The size of the LDPC code C1 is (4336, 3856) and the size of the SPC code C2 is (100, 99). The total code rate is 0.8804.

Fig. 4 shows the BER performance of the proposed decoding scheme with an LLR controller according to the SNR. When the AD is 2 Tb/in^2, the performance improvement of the proposed decoding scheme with an LLR controller is ~0.2 dB over that without an LLR controller at a BER of 10^{-5}. In addition, the performance of the proposed decoding scheme with an LLR controller is better than that of

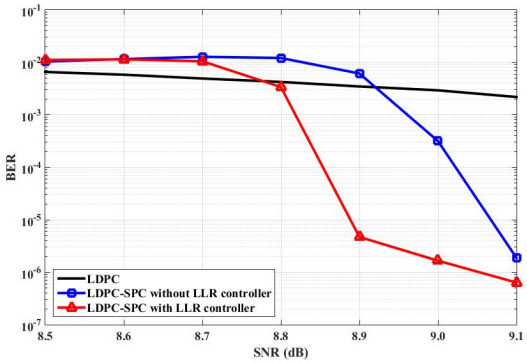

그림 4. LLR 컨트롤러를 사용한 곱 부호 디코딩 방식의 BER 성능
Fig. 4. BER performance of the proposed decoding scheme with LLR controller according to the SNR.

a conventional LDPC code. The iterative product decoding scheme with and without an LLR controller depends on the number of failed sectors and the SNR. Thus, in a low SNR region, the performance of the LDPC code alone is better than that of the iterative product decoding scheme with and without an LLR controller. However, in a high SNR region, the iterative product decoding scheme shows a better performance than LDPC codes alone.

Ⅴ. Conclusion

This paper proposed an iterative product coding scheme for bit-patterned media recording to improve the performance. The proposed product coding scheme consists of both an inner LDPC code to improve the error correction ability and an outer SPC code to increase the coding rate and flexibility. The proposed LLR controller scheme calculates the appropriate coefficients and modifies the LLR output of the LDPC decoder by exploiting the property of the syndrome. As the results indicate, the proposed iterative product decoding with the LLR controller scheme performs better than that without an LLR controller or an LDPC code alone. If an LLR controller is used in accordance with the system characteristics, a better performance can be achieved.

References

[1] T. R. Albrecht, et al., “Bit-patterned magnetic recording: Theory, media fabrication, and recording performance,” *IEEE Trans. Magn.*, vol. 51, no. 5, May 2015, Art. ID 0800342.

[2] H. J. Richter, A. Y. Dobin, O. Heinonen, K. Z. Gao, R. J. M. van de Veerdonk, R. T. Lynch, J. Xue, D. Weller, P. Asselin, M. F. Erden, and R. M. Brockie, “Recording on bit-patterned media at densities of 1 Tbit/in^2 and beyond,” *IEEE Trans. Magn.*, vol. 42, no. 10, pp. 2255-2260, Oct. 2006.

[3] R. L. White, R. M. H. Newt, and R. F. W. Pease, “Patterned media: A viable route to 50 Gbit/in^2 and up for magnetic recording?” *IEEE Trans. Magn.*, vol. 33, no. 1, pp. 990-995, Jan. 1997.

[4] R. Wood, M. Williams, A. Kavcic, and J. Miles, “The feasibility of magnetic recording at 10 terabits per square inch on conventional media,” *IEEE Trans. Magn.*, vol. 45, no. 2, pp. 917-923, Feb. 2009.

[5] S. Yang, Y. Han, X. Wu, R. Wood, and R. Galbraith, “A soft decodable concatenated LDPC code,” *IEEE Trans. Magn.*, vol. 51, no. 11, Nov. 2015, Art. no. 9401704.

[6] H. Saito, “Concatenated coding schemes for high areal density bit-patterned media magnetic recording,” *IEEE Trans. Magn.*, vol. 54, no. 2, Feb. 2018, Art. ID 3100210.

[7] C. D. Nguyen and J. Lee, “Elimination of two-dimensional intersymbol interference through the use of a 9/12 two-dimensional modulation code,” *IET Commun.*, vol. 10, no. 14, pp. 1730-1735, Sep. 2016.

[8] S. Jeong and J. Lee, “Performance of 8/10 modulation code according to areal densities on bit-patterned media recording,” *J. KICS*, vol. 44, no. 2, pp. 226-231, Feb. 2019.

[9] S. Nabavi, B. V. K. V. Kumar, J. A. Bain, C. Hogg, and S. A. Majetich, “Application of image processing to characterize patterning noise in self-assembled nano-masks for bit-patterned media,” *IEEE Trans. Magn.*, vol.

45, no. 10, pp. 3523-3526, Oct. 2009.

[10] D. Shin, K. Heo, S. Oh, and J. Ha, "A stopping criterion for low-density parity-check codes," in *Proc. IEEE 65th VTC Spring 2007*, pp. 1529-1533, Dublin, Ireland, Apr. 2007.

[11] M. P. C. Fossorie, M. Mihaljevic, and H. Imai, "Reduced complexity iterative decoding of low-density parity check codes based on belief propagation," *IEEE Trans. Commun.*, vol. 47, no. 5, pp. 673-680, May 1999.

정 성 권 (Seongkwon Jeong)

2015년 2월 : 숭실대학교 정보통신전자공학부 졸업

2017년 8월 : 숭실대학교 정보통신소재융합학과 석사

2018년 9월~현재 : 숭실대학교 정보통신소재융합학과 박사과정

<관심분야> 채널코딩, 스토리지시스템

[ORCID:0000-0002-4974-337X]

이 재 진 (Jaejin Lee)

1983년 2월 : 연세대학교 전자공학과 졸업

1984년 12월 : University of Michigan, Dept. of EECS 석사

1994년 12월 : Georgia Tech, Sch. of ECE 박사

1995년 1월~1995년 12월 : Georgia Tech, 연구원

1996년 1월~1997년 2월 : 현대전자 정보통신연구소 책임연구원

1997년 3월~2005년 8월 : 동국대학교 전자공학과 부교수

2005년 9월~현재 : 숭실대학교 전자정보공학부 교수

<관심분야> 통신이론, 채널코딩, 스토리지시스템

[ORCID:0000-0001-7791-3308]